Design ports and associated control circuits for a board named VME64x_BIU that is interfaced to the synchronous External Bus of the Freescale MPC563 Embedded Processor. A functional block diagram of the board is given on the next page. The schematic diagram should include the following:

- Local Bus address, data, and control line buffers (using 3.3V Low voltage Logic chips). Name the Local Bus signals LB_xx where xx is the normal MPC563 signal name, e.g. LB_A31,...,LB_A08, etc. Name the internal signals before/after buffering BIU_xx.

- Address decoder, registers and control logic to select the device being accessed through the MPC563 Bus and control the flow of data.

<table>
<thead>
<tr>
<th>Address Range (in hex)</th>
<th>Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>6000 0000 – 60FF FFFF</td>
<td>Dual Port SDRAM (32-bit port, 16Mbytes)</td>
</tr>
<tr>
<td>7000 0000 – 700F FFFF</td>
<td>VME64x Bus Data (32-bit port)</td>
</tr>
<tr>
<td>7010 0000 – 701F FFFF</td>
<td>VME64x Bus Address Latch (32-bit port)</td>
</tr>
<tr>
<td>7020 0000 – 702F FFFF</td>
<td>Reserved (32-bit port)</td>
</tr>
<tr>
<td>8000 0000 – 800F FFFF</td>
<td>VME64x Bus Addr. Mod. Latch (6-bit port)</td>
</tr>
<tr>
<td>8010 0000 – 801F FFFF</td>
<td>VME64x Interrupt Request (8-bit port)</td>
</tr>
<tr>
<td>8020 0000 – 802F FFFF</td>
<td>VME64x Interrupt Status (8-bit port)</td>
</tr>
</tbody>
</table>

- A synchronous state machine to deal with the timing issues of your design. You may assume that a 100MHz (50 % duty cycle) clock generator (asynchronous with respect to the MPC563 CPU clock) is available as a timing reference.

- Any glue logic should be implemented using the Xilinx XC2VP30 chip that is mounted on the XUPV2P Development Board.

In order to simplify your design the MPC 563 Processor interface is limited as follows:
- no bus arbitration signals
- no reservation and show cycle protocol signals
- no PTR and BI/STS signals
- no IRQ signals
- no signals associated with the embedded peripheral modules
- no internal TA signal programming

You may assume that the MPC563 clock rate is 40 MHz. You should utilize three programmable chip enable signals (CS1* - CS3*) of the MPC563 Processor. You should give the contents of the
relevant Memory Controller registers for your approach. You should assume that the MPC 563 CPU will access to the SDRAM, and the VME Bus space, respectively, using burst transfers only. The length of the burst transfers is limited to up to four beats. You may assume that the MPC563 External Bus Operates in Pre-Discharge Mode (3.3V – 5V signals are tolerated). The SDRAM and the VME64x ports should support dynamic bus sizing (i.e., byte, half-word, and word data), however, each data type is required to be properly aligned. If these condition are not met the selected memory range should respond by asserting the TEA* signal, rather than the TA* signal.

Design your TA* signal control logic such that your unit may respond to a MPC 563 bus cycle with 0, or, 1, or 2, or 4, or 8, or 16, or unlimited number of wait states, respectively, depending upon the needs of the selected memory range. No critical timing analysis is required for this project.

Tasks:

1. **Develop a .do file** to simulate a suitable set of MPC 563 bus cycles in order to verify the correct operation of your MPC 563 interface design.

2. Use VHDL and the Xilinx ISE tools along with ModelSim by Mentor Graphics to **design, simulate and implement your MPC 563 interface module**. Map the MPC 563 interface signals such that they will be accessible through the Hirose connector of the XUPV2P Development Board.

3. **Plot a schematic diagram** of your circuits. On the schematic, all nets must have labels and all devices must have distinct names- such as Uxx, where xx is a number, e.g., U00, etc.

4. **Demonstrate** the correct operation of you MPC 563 interface module by **simulation**. Use real-time (post-route) simulations.

5. Turn in a **Project Report**. Your Project Report should include the main sections as follows: Introduction, Design, and Conclusion.

The Class Web Page has pointers to relevant Data Sheets and User’s Manuals. Additional materials can be found on the Xilinx, Digilent and Freescale Home Pages, respectively, and on the other related manufacturers’ Web Pages.