

**Department of Electrical and Computer Engineering**

College of Engineering and Applied Sciences

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# **ECE 4510/5530**

# **Microcontroller Applications**

## **Miscellaneous Stuff**

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# Miscellaneous

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- MODE
  - Document S12MEBIV3

# Modes of Operation (1 of 2)

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- Normal Expanded Wide Mode
  - Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. This mode allows 16-bit external memory and peripheral devices to be interfaced to the system.
- Normal Expanded Narrow Mode
  - Ports A and B are configured as a 16-bit address bus and Port A is multiplexed with 8-bit data. Port E provides bus control and status signals. This mode allows 8-bit external memory and peripheral devices to be interfaced to the system.
- Normal Single-Chip Mode
  - There is no external expansion bus in this mode. The processor program is executed from internal memory. Ports A, B, K, and most of E are available as general-purpose I/O.
- Special Single-Chip Mode
  - This mode is generally used for debugging single-chip operation, boot-strapping, or security related operations. The active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. There is no external expansion bus after reset in this mode.

# Modes of Operation (2 of 2)

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- **Emulation Expanded Wide Mode**
  - Developers use this mode for emulation systems in which the users target application is Normal Expanded Wide Mode.
- **Emulation Expanded Narrow Mode**
  - Developers use this mode for emulation systems in which the users target application is Normal Expanded Narrow Mode.
- **Special Test Mode**
  - Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.
- **Special Peripheral Mode**
  - This mode is intended for Motorola factory testing of the system. The CPU is inactive and an external (tester) bus master drives address, data, and bus control signals.

# MODE Setting

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- BKGD/MODC/TAGHI
  - At the rising edge on RESET, the state of this pin is registered into the MODC bit to set the mode. (This pin always has an internal pullup.)
- PE6/IPIPE1/MODB/CLKTO
  - At the rising edge of RESET, the state of this pin is registered into the MODB bit to set the mode.
- PE5/IPIPE0/MODA
  - At the rising edge on RESET, the state of this pin is registered into the MODA bit to set the mode.

# MODE Register

Address: Base + \$\_0B

|        | BIT 7 | 6    | 5    | 4 | 3    | 2 | 1   | BIT 0 |                              |
|--------|-------|------|------|---|------|---|-----|-------|------------------------------|
| Read:  | MODC  | MODB | MODA | 0 | IVIS | 0 | EMK | EME   |                              |
| Write: |       |      |      |   |      |   |     |       |                              |
| Reset: | 0     | 0    | 0    | 0 | 0    | 0 | 0   | 0     | Special Single Chip          |
| Reset: | 0     | 0    | 1    | 0 | 1    | 0 | 1   | 1     | Emulation<br>Expanded Narrow |
| Reset: | 0     | 1    | 0    | 0 | 1    | 0 | 0   | 0     | Special Test                 |
| Reset: | 0     | 1    | 1    | 0 | 1    | 0 | 1   | 1     | Emulation<br>Expanded Wide   |
| Reset: | 1     | 0    | 0    | 0 | 0    | 0 | 0   | 0     | Normal Single Chip           |
| Reset: | 1     | 0    | 1    | 0 | 0    | 0 | 0   | 0     | Normal<br>Expanded Narrow    |
| Reset: | 1     | 1    | 0    | 0 | 0    | 0 | 0   | 0     | Peripheral                   |
| Reset: | 1     | 1    | 1    | 0 | 0    | 0 | 0   | 0     | Normal<br>Expanded Wide      |

= Unimplemented

**Figure 3-10 MODE Register (MODE)**

If MODC = 1, MODB = 0, and MODA = 0, then MODC is write never. MODB and MODA are write once, except that you cannot change to special peripheral mode. From normal single-chip, only normal expanded narrow and normal expanded wide modes are available.

# Access E-Clock on PE.4


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- Port E serves as general-purpose I/O or as system and bus control signals.
- The PEAR register is used to choose between the general-purpose I/O function and the alternate control functions.
- When an alternate control function is selected, the associated DDRE bits are overridden.

# Port E Assignment Register

Address: Base + \$\_0A

|        | BIT 7  | 6 | 5     | 4     | 3     | 2    | 1 | BIT 0 |                           |
|--------|--------|---|-------|-------|-------|------|---|-------|---------------------------|
| Read:  | NOACCE | 0 | PIPOE | NECLK | LSTRE | RDWE | 0 | 0     |                           |
| Write: |        |   |       |       |       |      |   |       |                           |
| Reset: | 0      | 0 | 0     | 0     | 0     | 0    | 0 | 0     | Special Single Chip       |
| Reset: | 0      | 0 | 1     | 0     | 1     | 1    | 0 | 0     | Special Test              |
| Reset: | 0      | 0 | 0     | 0     | 0     | 0    | 0 | 0     | Peripheral                |
| Reset: | 1      | 0 | 1     | 0     | 1     | 1    | 0 | 0     | Emulation Expanded Narrow |
| Reset: | 1      | 0 | 1     | 0     | 1     | 1    | 0 | 0     | Emulation Expanded Wide   |
| Reset: | 0      | 0 | 0     | 1     | 0     | 0    | 0 | 0     | Normal Single Chip        |
| Reset: | 0      | 0 | 0     | 0     | 0     | 0    | 0 | 0     | Normal Expanded Narrow    |
| Reset: | 0      | 0 | 0     | 0     | 0     | 0    | 0 | 0     | Normal Expanded Wide      |

 = Unimplemented

**Figure 3-9 Port E Assignment Register (PEAR)**

# Setting NECLK

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- NECLK — No External E Clock
  - Normal and Special: write anytime
  - Emulation: write never
  - 1 = The associated pin (Port E, bit 4) is a general-purpose I/O pin.
  - 0 = The associated pin (Port E, bit 4) is the external E clock pin.  
External E clock is free-running if ESTR = 0
  - External E clock is available as an output in all modes.
- The bit must be cleared in order to see E-Clock
  - `PEAR &= ~NECLK;`

# Background Debug Module

- **BKGD/MODC/TAGHI**
  - Pseudo open-drain communication pin for the single-wire background debug mode. There is an internal pull-up resistor on this pin.
  - From S12MEBIV3
- Describe in S12BDMV4

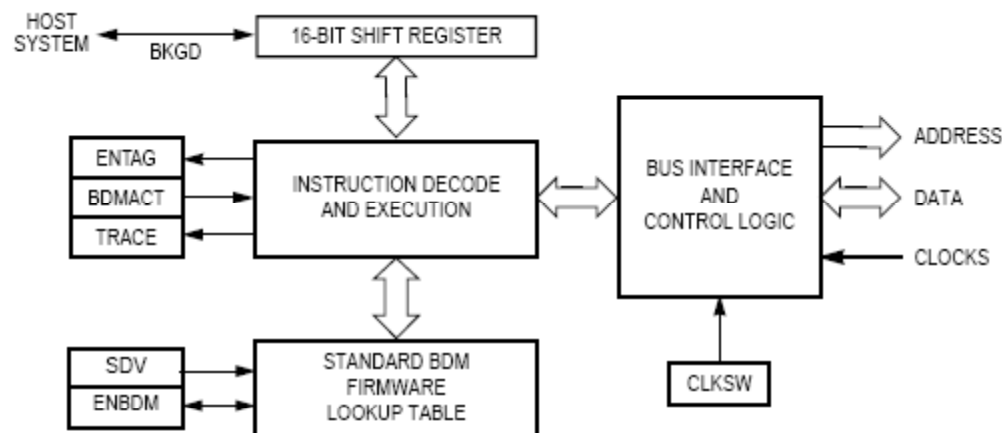


Figure 1-1 BDM Block Diagram

# BDM

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- Bypasses other pins and code operation
- Allows direct access to registers and memory
- When Debug12 was “not right”
  - Load (flash) a boot loader using the BDM
  - Switch to the boot loader program running through the SCI0 port
  - Load (flash) the desired program.
- One HCS12 Module can act as a BDM for another!