

Lecture Outline
(Tentative)

<i>Topic</i>	<i>Reading Assignment</i>
Combinational logic design in VHDL, CPLDs, FPGAs, Xilinx and Mentor Graphics tools	Notes, Home Page, Xilinx and MG Web sites 2.1-2.4, 2.15, 3, 4.1-4.3
VHDL programming examples (combinational logic)	VHDL Tutorial, Home Page
Time faults in combinational logic circuits	Notes, Sandige, Nelson 1.5
Stuck-at-faults in combinational logic	Notes
Interface devices (O.C., TS)	Notes
Finite state machine (FSM) models	Notes
Synchronous design with state machines, ASM method	Notes, Wakerly
State machine design with in VHDL, CPLDs, FPGAs, Xilinx and Mentor Graphics tools	Notes, Home Page, Xilinx and MG Web sites 2.5-2.7, 4.4-4.7, 5
VHDL programming examples (sequential logic)	VHDL Tutorial, Home Page
Analysis of synchronous finite state machines	Notes, Wakerly, Sandige
Clock skew and asynchronous inputs	Notes, Wakerly
Microprogrammed system controllers	Notes
Analysis and synthesis of asynchronous sequential machines, timing hazards in asynchronous circuits	Notes, Sandige, Nelson, Home Page
Design of asynchronous sequential machines in VHDL	Notes, Home Page
Introduction to microprocessor-based digital systems design	Notes
Interfacing to intelligent I/O devices	Notes
DRAM chips, design issues of DRAM memory systems	Notes, Home Page