

ECE 3550 P#2 Demo

Student Name	8-char custom ID	<u>Comments</u>
		<ul style="list-style-type: none"> - circuit is fully assembled: - config file is downloaded: - S35 is operational: (no CLK!)

Tests

- D-BUS
D7-D0 LEDs when $CE^* = 1 \wedge RD^* = 0$, $CE^* = 0 \wedge RD^* = 1$

- Mode 0 input
 - load CR.0 = CR.1 = 0 ($CE^* = 0, AO = 1, WR^* = \downarrow$)
 - peripheral data read & transparency test
 $CE^* = 0, AO = 0, RD^* = 0$ P7-P0 = 0x5A
 - check D7-D0, change Px bits
 - $RD^* = 1$, check transparency again

- Mode 1 input, interrupt is enabled
 - $STB^* = 1$
 - load CR.0 = CR.1 = 1 ($CE^* = 0, AO = 1, WR^* = \downarrow$)
 - read status register ($CE^* = 0, AO = 1, RD^* = \downarrow$)
while $RD^* = 0$, D2-D0 = 010
 - peripheral loads data ($STB^* = \downarrow$ P7-P0 = 0xC3
($CE^* = 1!$))
 - read status register
($CE^* = 0, AO = 1, RD^* = \downarrow$ - D2-D0 = 111)
IBF & INTR shouldn't change)
 - read data & transparency test
($CE^* = 0, AO = 0, RD^* = \downarrow$ D7-D0 = 0xC3)

- Mode 1 input, INTB = 0

