ECE 3550 DIGITAL DESIGN

FALL 2011

Project Assignment #2

(Team Project)

Total: 40 pts. (10% of course grade)

Due 4:00pm, Thursday, December 8, 2011

Design, **simulate**, **implement**, and **demonstrate** a **Parallel I/O chip (PIO)** specified below. Use one **Xilinx XC3S500-FG320 SPARTAN-3E FPGA** chip (or if it is different, the chip that is actually mounted on your Nexys 2 Board), DIP-switches, bounce-free switches, Bar-LED modules, and various buffer chips, as needed. The states of the input signals are to be set by switches, and outputs are to be displayed using LEDs. The switches representing microprocessor data output signals should be separated from the PIO's Three-State (TS), bi-directional bus signals by a TS buffer chip. The LEDs should be driven by inverting-output buffers to provide for a true display of the status of the signals. You must provide for your own parts.

Functionally, this PIO can be viewed as a **segment** of the **Intel i82C55A** chip (refer to Intel's Web site, or any recent Intel Peripheral Components Handbook for further readings). The microprocessor interface signals are as follows: **CE*, A0, RD*, WR*, RESET,** and **INTR** (* stands for active-low), as well as **D0,...,D7** (bi-directional TS data bus lines). On the peripheral interface, **just one 8-bit data input port P0,...,P7** should be implemented along with supporting hand-shake signals **STB***, and **IBF**. The key control signals of the PIO chip (CE*, RD*, WR*, and STB*) should be driven by **bounce-free** switches.

The **register model** of your PIO chip consists of three registers: **Data_In (selected by A0 = 0, for read access only)**, **Control_Reg (A0 = 1, for write access only)**, and **Status_Reg (A0 = 1, for read access only)**. **<u>These registers are accessed while both CE* and the required control signal (RD*, or WR*, respectively) are asserted along with the particular value of A0 as specified above</u>.**

The **bit maps** of these registers and their functions are as follows:

Control_Reg.0: MODE Bit
if 0: Mode 0 input from peripheral
if 1: Mode 1 input from peripheral
Control_Reg.1: INTE (Interrupt Enable) Bit
if 1: signal INTR is enabled
if 0: INTR is disabled

Status_Reg.0: IBF (Input Buffer Full) Bit
Status_Reg.1: INTE (Interrupt Enable) Bit
Status_Reg.2: INTR (Interrupt Request) Bit

Signal **RESET** resets **all control** and **status register bits**, and the **INTR signal** to **0** when it is asserted. RESET is **active-high**.

The basic **timing diagrams** for the peripheral and microprocessor interface signals are given on Page 3. You are **NOT required** to implement the **exact delay times** given in the i82C55A Data Sheets but the **antecedent - consequent** relationship between handshake pairs of signals, instead. For your orientation, research the Xilinx Web site for information on the SPARTAN-3E chips. A link is provided in the Data Sheets Section of the Class Web Page.

Tasks:

a) Give a **narrative summary** along with a **detailed schematic diagram** of your circuit. In the schematics, represent the SPARTAN-3E chip by a rectangular block with signal names assigned to the appropriate pins. Also **show the detailed design steps (i.e., primitive flow map, reduced state table, assigned state table, logic functions) for the asynchronous sequential logic section** of your circuit along with your **comments**. (6 pts.)

b) **Design, simulate and implement** the circuits that should be mapped to your SPARTAN-3E FPGA. You should design your circuits in VHDL and use the current Xilinx ISE tools to implement your chip. You should also carry on **post-route simulations** using **.do** files to evaluate the **real-time** performance of your design.
Comment on your simulation results. Attach hard copies of your **.vhd**, and **.do** files, your simulation **timing diagrams with comments**, as well as the pin assignment and the resource utilization sections of the **Pad Report**. (18 pts.)

c) **Download** your **.bit** file to the SPARTAN-3E chip on your Nexys 2 Board. Hook up the board to the rest of your circuit you have built on your Breadboard.
Demonstrate the correct operation of your PIO chip. (16 pts.)

Each team should submit a **joint Project Report**. In the report, you should have sections as follows: Introduction, Design, and Conclusion. **You lose 4 pts.** (10%) **by each day the project is tardy**. **No credit** will be given if the project is **late by more than 5 days**.