

ECE 3550 DIGITAL DESIGN
FALL 2011
Bonus Assignment to Project #2
Total: 16 pts. (4% of course grade)
Due 4:00pm, Thursday, December 8, 2011

This Bonus Assignment is an **extension to the Project #2 specifications**. In essence, it doubles the functionality of the 8-bit peripheral data port by adding **Mode 0, and Mode 1 Output**, respectively, to the Parallel I/O (PIO) chip. A revised specification is given below. **Bold** typeface indicates **new** specs.

Functionally, this PIO chip can be viewed as a segment of the Intel i82C55A chip (refer to Intel's Web site, or any recent Intel Peripheral Components Handbook for further readings). The microprocessor interface signals are as follows: CE*, A0, RD*, WR*, RESET, and INTR (* stands for active-low), as well as D0,...,D7 (bi-directional TS data bus lines). On the peripheral interface, **depending on the programming of the Control_Reg register**, just one **8-bit data input port, or output port (P0,...,P7)**, respectively, should be implemented along with hand-shake signals STB*, IBF, **OBF***, and **ACK***. The critical control signals (CE*, RD*, WR*, STB*, and **ACK***) should be driven by bounce-free switches. Signals P0,...,P7 are technically **not bi-directional** because **the peripheral port can only be configured as either input, or output** (mutually exclusive) for a **given session** as determined by the **contents** the control register Control_Reg.

The register model of the PIO consists of **four** registers: **Data_Out** (selected by **A0=0, for write access only**), Data_In (A0=0, for read access only), Control_Reg (A0=1, for write access only), and Status_Reg (A0=1, for read access only). These registers are accessed while both CE* and the required control signal (RD*, or WR*, respectively) are asserted along with the particular value of A0 as specified above.

The bit maps of these registers and their functions are as follows:

Control_Reg.0: MODE Bit (**either Input, or Output** as determined by **Bit 2**)

if 0: Mode 0

if 1: Mode 1

Control_Reg.1: INTE (Interrupt Enable) Bit

if 1: signal INTR is enabled

if 0: INTR is disabled

Control_Reg.2: DIR (Direction) Bit

if 0: Output

if 1: Input

Status_Reg.0: IBF (Input Buffer Full) Bit

Status_Reg.1: INTE (Interrupt Enable) Bit

Status_Reg.2: INTR (Interrupt Request) Bit

Status_Reg.3: OBF* (Output Buffer Full) Bit

Signal RESET resets all control and status bits and the INTR signal to 0, and also **sets bit DIR to 1** when it is asserted. RESET is **active-high**. The **additional timing diagrams** for the peripheral and microprocessor interface signals are given on Page 3, on the Class Web Page. You are not required to implement the exact delay times given in the i82C55A Data Sheets but the antecedent – consequent relationship between pairs of handshake signals, instead. For your orientation, research the Xilinx Web site for information on the SPARTAN-3E chips.

Tasks:

- a) Give a narrative summary along with a detailed schematic diagram of your circuit. In the schematics, represent the SPARTAN-3E chip by a rectangular block with signal names assigned to the appropriate pins. Also show the detailed design steps (i.e., primitive flow map, reduced state table, assigned state table, logic functions) for the asynchronous sequential logic section of your circuit along with your comments. (4 pts.)
- b) Design, simulate and implement the circuits that should be mapped to your SPARTAN-3E FPGA. You should design your circuits in VHDL and use the current Xilinx ISE tools to implement your chip. You should also carry on post-route simulations using .do files to evaluate the real-time performance of your design.
Comment on your simulation results. Attach hard copies of your .vhd, and .do files, your simulation timing diagrams with comments, as well as the pin assignment and the resource utilization sections of the Pad Report. (6 pts.)
- c) Download your .bit file to the SPARTAN-3E chip on your Nexys 2 Board. Hook up the board to the rest of your circuit you have built on your Breadboard.
Demonstrate the correct operation of your PIO chip. (6 pts.)

This Bonus Project can be demonstrated only **after** the basic one. Each team should submit a joint Project Report. In the report, you should have sections as follows: Introduction, Design, and Conclusion. **You lose 1.6 pts. (10%) by each day the project is tardy. No credit** will be given if the project is **late by more than 5 days**.