

ECE 3550 Digital Design Required Course

2008-2009 Catalog Data:

ECE 3550: Digital Design
Systems level design of digital logic circuits using hardwired and programmable system controllers. Introduction to asynchronous sequential logic circuits.
Credit: 4 hours
Prerequisite: ECE 2500

- Textbook(s) and/or Required Materials:**
1. Charles H. Roth, Jr, Lizy Kurian John, Digital Systems Design Using VHDL, Second Ed., Thompson Learning, 2008, ISBN 10 0-534-38462-5, available in the University Bookstore, Bernhard Center
 2. Materials disseminated using the [ECE 3550 Class Web Page](#) (the official media for the class)
 3. ECE 3550 Parts Kit
 4. Current Xilinx WebPack along with ModelSim MXE

Recommended Materials:

1. Instructor's Lecture Notes
2. R. S. Sandige, *Modern Digital Design*, McGraw-Hill, 1990
3. J. F. Wakerly, *Digital Design, Principles and Practices*, Third Edition, Prentice-Hall, Inc., 2000, ISBN 0-13-769191-2

References:

1. Data Sheets of selected CPLDs and Spartan3E FPGAs are available through the Xilinx Web site
2. FPGA/PLD CAD materials are available through the Xilinx and MG Web sites

Coordinator:

Dr. Janos L. Grantner, Professor of Electrical and Computer Engineering

Instructor in the Fall 2008 Semester:

Dr. Janos L. Grantner

Prerequisites by topic:

1. Introductory level digital logic design
2. Knowledge of a PLD programming language

Course Objectives: (ABET Learning Outcomes)

1. To provide experience to analyze, design, simulate and experimentally validate combinational logic circuits using Programmable Logic Devices (CPLDs and FPGAs) (a, b, c, e)
2. To provide experience to analyze, design, simulate and experimentally validate system control units based upon synchronous sequential circuits and using Programmable Logic Devices (CPLDs and FPGAs) (a, b, c, e)
3. To provide experience to analyze, design, simulate and experimentally validate system control units based upon asynchronous sequential circuits and using Programmable Logic Devices (CPLDs and FPGAs) (a, b, c, e)
4. To provide experience to utilize contemporary circuit synthesis and simulation software tools (k)
5. To provide experience to use electronic test instrumentation to validate and debug digital systems (k)
6. To develop skills to prepare effective written technical communications for engineering analysis and design work through project reports (g)
7. To assess the students' sense of ethical and professional responsibility (f)
8. To assess the students' knowledge on contemporary issues (j).

Topics:

1. Course overview, introduction, and documentation system for combinational logic design (1 class)
2. Variable-entered maps (VEM) (2 classes)
3. Time faults in combinational logic circuits (2 classes)
4. Stuck-at-faults in combinational logic (1 class)
5. Architecture of CPLDs, design of combinational logic circuits using VHDL and ModelSim (5 classes)
6. Finite state machine models (1 class)
7. Synchronous sequential circuit analysis and synthesis (5 classes)
8. Synchronous design with state machines, the ASM method (1 class)
9. Use of VHDL and ModelSim to design and simulate synchronous FSMs (4 classes)
10. Impediments to synchronous logic circuit design (2 classes)
11. Programmable (microcoded) system controllers (2 classes)
12. Analysis and design of asynchronous sequential machines, hazards in asynchronous circuits (5 classes)
13. Use of VHDL and ModelSim to design and simulate asynchronous sequential logic circuits (2 classes)
15. Digital design using FPGAs (2 classes)
15. Introduction to microprocessor-based digital systems design, interfacing I/O devices (4 classes)
16. Important types of interface devices (O.C., TS), guidelines to microprocessor systems design (1 class)
17. Introduction to Projects (2 classes)
18. Test (1 class)

Course/Laboratory Schedule: 3 one-hour lectures and a 3-hour laboratory

Evaluation:

1. Examinations (50%)
2. Design Projects (20%)
3. Laboratory(20%)
4. Homework (10%)

Design Projects:

Design, build, and demonstration of a simple, synchronous, serial arithmetic unit (a bonus project is also offered, 4 weeks). A report is required.

Design, build, and demonstration of an asynchronous, programmable, parallel I/O chip (a bonus project is also offered, 4 weeks). A report is required.

Computer Usage:

Xilinx ISE/WebPack 10.1i CAD software and ModelSim 6.4 by Mentor Graphics are used to carry out the design and simulation steps of the projects, and to work on selected homework assignments.

Contribution to Professional Component:

ABET professional component content as estimated by faculty member who prepared this course description:

Engineering sciences:	1 credit or 33%	Engineering design:	2 credits or 66%
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Relation of Course to Program Outcomes:

This course provides significant support for the CE program objectives Depth and Professionalism along with learning outcomes a, b, c, e, g and k.

Prepared by: Dr. Janos L. Grantner

Date: September 7, 2008