

Review for the Midterm Exam

The Midterm Exam will be given 11:30am-12:20pm, on Monday, October 17, 2011, in class (Room D-206). It will be a problem-oriented, open text book (Charles H. Roth, Jr. and Lizy Kurian John, Digital Systems Design Using VHDL, 2nd Ed., Thompson, 2008) but no notes test. The use of laptops, PDAs and cell phones are strictly prohibited. Students should bring their Blue/Green Exam Pads to the exam. Students are responsible for topics covered in class in the labs and in the homework assignments.

Topics covered in class include:

Active-H and Active-L logic signals

Timing diagrams

Static, dynamic and function hazards in combinational logic circuits

- analysis of combinational logic circuits for hazards
- design of hazard-free circuits

Stuck-at faults and bridging faults in combinational logic circuits

- devising test vectors to detect faults

Design of combinational logic circuits using VHDL and PLDs

- WebPack and ModelSim, Xilinx FPGAs and CPLDs
- VHDL files and simulation macro files

Synthesis of synchronous sequential circuits (NOT AN EXAM TOPIC!)

- Mealy and Moore models of synchronous sequential circuits
- state machines
- ASM charts
- design of synchronous sequential circuits using VHDL and PLDs
- VHDL files and simulation macro files