SOLUTIONS TO MT EXAM #1

1. [10 pts]) Define, describe or provide a short answer:

(a [2pts]) List the five RISC design principles.

p. 59-61.

All instructions are directly executed by hardware
Maximize the rate at which instructions are issued
Instructions should be easy to decode
Only loads and stores should reference memory
Provide plenty of registers

(b [2 pts]) What are cache locality principles and why are they important?

p. 78-79.

Caches store data that possesses certain locality principles, such as temporal, sequential and spatial locality. Data and instructions tend to have these properties, which means that a small, fast cache memory can hold a high percentage of the address references that will occur and thereby reduce the average memory access time.

(c [2 pts]) What is a tri-state gate or device and why is it important in computers?

p. 167-168.

A tri-state is gate is capable of three output states, a 0, a 1 or high impedance/open circuit.

They are required whenever multiple signal paths can drive a common line or bus. If the tri-state does not operate correctly multiple signals may be driven simultaneously resulting in incorrect signal levels, a potential shorting of the power to ground through the gates, and likely permanent damage to the circuit.

(d [2 pts]) Why might it be difficult to tell in a multilevel machine if a program is being translated or interpreted? If execution time is a concern, why might the programmer/engineer want to know?

p. 4.

A person whose job it is to write programs for a level n machine need not be aware of the underlying interpreters and/or translators. If fast program operation is required, interpretation is not desirable, it will make program execution relatively slower.
(e [2 pts]) Describe the difference between a gated D-latch and a clocked D-flip-flop.

p. 161-163.

The gated device will allow the input to propagate to the output during the entire time that the gate is enabled. Once the gate is removed, the output will remain stable until the gate opens again.

The clocked device will only collect the D-input present when the clock event happens (e.g., the rising edge) and will propagate and maintain it at the output until the next clock occurs.

2. [18 pts]) Perform the following row operations on each of the equations given. For addition, report overflow if it occurs.

Integer Arithmetic:

4-bit unsigned addition to generate a 4-bit result with overflow status and
4-bit 2’s complement addition to generate a 4-bit result with overflow status and
4-bit 2’s complement multiplication to generate an 8-bit result.

<table>
<thead>
<tr>
<th>Equation</th>
<th>0011 0100</th>
<th>1010 1101</th>
<th>0110 1001</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unsigned Addition</strong></td>
<td>0111</td>
<td>(ovf) 0111</td>
<td>1111</td>
</tr>
<tr>
<td><strong>2’s Comp Addition</strong></td>
<td>0111</td>
<td>(ovf) 1-0111</td>
<td>1111</td>
</tr>
<tr>
<td><strong>2’s Comp Multiply</strong></td>
<td>0000 1100</td>
<td>0001 0010</td>
<td>1101 0110</td>
</tr>
</tbody>
</table>
3. [10 pts]) Assume that we have a 96 gigabyte hard disk (use exactly $3 \times 2^{35}$ bytes). It consists of three platters with six surfaces with 512 sectors per track. Assume that the platters are aligned and can be simultaneously read or written. The disk rotates at 7200 RPM with an average seek time of 12.5 msec.

(Note: use 1 kB=1024 B, 1 MB = 1024 kB, and 1 GB = 1024 MB)

(a [4 pts]) What is the average data read or write rate in MBytes/second for the disk. (include the average seek time, the average rotational latency, and the simultaneous read/write of 6 surfaces at the cylinder location)

$$2^9 \text{ sectors/track} \times 2^9 \text{ bytes/sector} = 2^{18} \text{ bytes/track}$$

$$7,200 \text{ RPM} / 60 \text{ sec/M} = 120 \text{ rev/sec}$$

$$T= 0.0125 \text{ sec} + 0.5/120 \text{ sec} + 1/120 \text{ sec} = 0.0125 + 0.00417 + 0.00833 = 0.025 \text{ sec}$$

Transfer rate $= 6 \text{ tracks} \times 2^{18} \text{ bytes/track}/T = 1,572,864 B/0.025 \text{ sec} = 62,914,560 B/sec$

Or $60.00 \text{ MB/sec}$

(b [3 pts]) For a digital data CD (mode 1) running on an 24x writer, what is the data transfer rate (in Bytes/sec) ?

p. 95-97.

Digital, Mode 1 is 153,600 B/sec whereas Audio, Mode 2 is 175,200 B/sec

$$153,600 \text{ B/sec} \times 24 = 3,686,400 \text{ B/sec} \text{ or } 3.51 \text{ MB/sec}$$

(c [2 pts]) How many single-sided, single-layer CDs would be required to store the contents of the above hard disk?

p. 95-97.

Single-sided, single-layer Mode 1 data CD 681,984,000 Bytes

$$3 \times 2^{35} \text{ bytes} / (666,000 \times 2^{10} \text{ bytes}) = 151.146 \text{ CDs}$$
(d [1 pt]) How long does it take the CD of part (b) to write one (1) sec of data from the hard disk at the average rate determined in part (a)?

\[
62,914,560 \text{ B/sec} \div 3,686,400 \text{ B/sec} = 17.067 \text{ sec}
\]

4. [20 pts]) The memory map for a microcontroller consists of a 64 kB memory space. The processors has five distinct regions, one for a memory mapped register file, one for an EPROM containing the program, one for FLASH programmable EEPROM non-volatile memory storage, one for static RAM for variables and computation, and one for memory-mapped input/output peripheral devices.

The EPROM requires 16 kB of space and must start a address 8000 hex, the Flash EEPROM requires 16 kB of space, the memory mapped register file requires 1 kB and must start at 0000 hex, the RAM requires 8 kB of space, and the PIO region consists of a 4 kB region.

(a [8 pts]) Plan and layout the memory-map similar to the text example in Figure 3-61 on p. 223.

Use the following address space structure.

<table>
<thead>
<tr>
<th>Reg File: 0000 to 03FF (msb 000)</th>
<th>PIO: 2000 to 1FFF (msb 001)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPROM: 8000 to BFFF (msb 10)</td>
<td>FLASH: C000 to FFFF (msb 11)</td>
</tr>
<tr>
<td>RAM: 4000 to 5FFF (msb 01)</td>
<td></td>
</tr>
</tbody>
</table>

![Memory Map Diagram](image-url)
(b [12 pts]) Provide the address decoding logic required for each of the memory spaces defined in part (a) above. Your designs should be similar to those in Figure 3-62(a) on p. 224.

Please note that the CS logic shown below is active-High. It capitalizes on the available unused memory blocks to simplify the logic needed.
5. [12 pts]) High end graphics video data transfer over a PCI bus. Assume that a high end graphics card is going to be designed to connect to the PCI bus. The specification needs to define the amount of memory on the graphics card and the percent utilization of the PCI bus. 

(Note: use 1 kB=1024 B, 1 MB = 1024 kB, and 1 GB = 1024 MB)

(a [5 pts]) Assume that the high end graphics card is going to support a 1280 x 960 pixel display. For graphics, the card provides 4 pixel memory buffers, each supporting 3-byte RGB color. How much RAM is required on the graphics card?

| columns x rows | 1280 x 960 =1,228,800 pixels |
| pixels * 4 buffers * 3 Bytes/pixel. | 1,228,800 * 4 * 3 =14,745,600 B |
| | = 14,400 kB |
| | = 14.06 MB |

(b [2 pts]) Assume that the graphics card displays 30 frames per second (each frame is one full pixel memory buffer). If a CPU is to provide this data, what is the transfer rate required?

| Pixels/frame * 3 Bytes/pixel * 30 frames/sec | 1,228,800 * 3 * 30 = 110,592,000 B/sec = 108 kB/sec = 105.47 MB/sec |

(c [3 pts]) A PCI bus is capable of block or burst write transfers, similar to that shown in Fig. 3-42, but using the write timing of Fig. 3-56. If the writes are performed as 32 Byte block transfers over a 66 MHz, 64-bit PCI bus, what is the transfer rate?

(Note: clock rates MHz are in 10^6 Hz)

| 64-bits = 8B |
| 32 B/ 8B per write cycle = 4 write cycles |

| 3cycles for 1 write → 6 cycles for 2 write |

| 66 MHz x 8 B/BusCycle x 4 BusCycle/transfer / (3+3) cycles/transfer = 352,000,000 B/sec. |
| = 335.69 MB/sec |

(d [2 pts]) What percentage of the transfer rate does writing frames of pixel memory require? (This is one reason why graphics is not typically done over a PCI bus anymore.)

| 110,592,000 B/sec / 352,000,000 B/sec = 31.42% |
6. [12 pts])

(a [2 pts]) If the Big Endian code word 32 0 48 1 is transferred to a Little Endian machine, the result will be

\[ \_1\_ \_48\_ \_0\_ \_32\_ \]

(b [6 pts]) A 7-bit Hamming code for the data word 0011 is:

\[ \_0\_ \_0\_ \_1\_ \_1\_ \_1\_ \_0\_ \] (show your calculations)

\[ I_4I_3I_2I_1 = 0011 \]
\[ C_3 \text{ XOR } 1 \text{ XOR } 0 \text{ XOR } 0 = 0 \quad C_3 = 1 \]
\[ C_2 \text{ XOR } 1 \text{ XOR } 0 \text{ XOR } 0 = 0 \quad C_2 = 1 \]
\[ C_1 \text{ XOR } 1 \text{ XOR } 1 \text{ XOR } 0 = 0 \quad C_1 = 0 \]
\[ I_4I_3I_2C_3I_1C_2C_1 = 0011110 \]

(c [2 pts]) To correct 3 single bit errors requires a _7_ - bit Hamming distance code.

\[ 2d + 1 = 7 \]

(d [2 pts]) _snooping_ is the word which describes how one processor looks for references to words on the memory bus that have been cached by another processor.