

ECE 4500/5540 DIGITAL ELECTRONICS

FALL 2011

Project Assignment #1 - Bonus

(Team Project)

Total: 16 pts. (4% of course grade)

Due 3:00pm, Friday, November 4, 2011

Demonstrations in the B-214 Lab

Specifications:

They are essentially the same as those for Project #1 but **additional functions** must also be implemented. Bit **CC3** is added to the Command Code in order to accommodate the new functions along with the standard ones. The **extended** function chart of the ALU is given below.

<u>Command Code CC</u>				<u>Function F</u>
CC3	CC2	CC1	CC0	
0	0	0	0	A
0	0	0	1	NOT(A)
0	0	1	0	A AND B
0	0	1	1	A OR B
0	1	0	0	A XOR B
0	1	0	1	A PLUS B w/o Carry
0	1	1	0	A MINUS B w/o Borrow
0	1	1	1	B
1	0	0	0	Logic Shift Left A (LSLA)
1	0	0	1	Logic Shift Right A (LSRA)
1	0	1	0	Arithmetic Shift Left A (ASLA)
1	0	1	1	Arithmetic Shift Right A (ASRA)
1	1	0	0	0000
1	1	0	1	A PLUS B with Carry (CIN is an input variable)
1	1	1	0	A MINUS B with Borrow (BW is an input variable)
1	1	1	1	B PLUS 1

The **three new arithmetic** operations and the **two arithmetic shift** operations, respectively, affect **all** flag outputs (you **don't** need to implement any flag register bits at this time, though). For the **two logic shift** operations **OVF must be set to 0**, the **other three flags are affected**. In case of the **F = 0000** operation **OVF must be set to 0**, the status of **S**, **Z** and **COUT** is irrelevant. For the **shift** operations the input bit is always a 0 but for the ASRA for which it is the status of the most significant bit (A3). **Output Carry** should show the status of the bit that is shifted out. Add (Subtract) with Carry (Borrow) allows arithmetic operations to be executed on operands of **extended length**. The status of the initial Carry (Borrow) would be determined by the Carry Flag set by the previous Add (Subtract) operation. However, since you won't implement flag flip-flops in this project, input CIN/BWIN should be driven by the simulator. You can choose **any**

design style for CMOS logic. Only **non-complemented** input signals are available. The terminal configuration of the layout should allow access to all input signals from the top, and all output signals from the bottom of the cell. The power lines should be on first-layer metal rails that pass completely through the cell in a horizontal direction. Use W/L ratios for your transistors such that the circuit outputs will exhibit near minimum average propagation delays. You are going to work with a 0.25-micron CMOS technology, however, the minimum feature size (L_{MIN}) should not be less than 1.2 μm and W_{MIN} is 2.0 μm .

Tasks:

1. Give a **discussion** of the **main points** of your design.
2. Develop a **transistor-level schematics** for each symbol using **Design Architect**. Turn in a hard copy of the symbol-level **schematic diagram** of your circuit. In addition, give the **total transistor count**.
3. **Verify the correct operation** of your circuit using **Eldo and Zelga**. You should also obtain the **VTC** for **one F** output bit of your choice, as well as the **worst case t_{PLH}** and **t_{PHL}** delay times for the **whole** circuit, and the average delay **t_{p}** . Plot your **simulation results** and **comment** on them.
4. **Design a layout** for your circuit using **Icstation**. Give the **size of area** of a rectangle that confines your design. Turn in a hard copy of the **layout diagram**.
5. Perform the **Parasitic Extraction of the layout using Calibre xRC**
6. Give the **product** of the **area**, **t_{PLH}** , and **t_{PHL}**
7. **Demonstrate** the working project to the Lab Instructor (a **separate** demo with respect to the standard project demonstration).

Submissions:

Project Report (hard copy) that includes:

- a) Introduction
- b) Discussion of your design
- c) Transistor-level and symbol-level schematic diagrams
- d) Simulation timing diagrams along with comments
- e) Final specs of your circuit (size of area, and area-delays product included)
- f) Printout of the Mentor layout
- g) Conclusions

Each Team must submit a **joint** Project Report that is **separate** from the standard project report.

Note: you will lose 1.6 pts. by each day your bonus project is tardy. **No** credit will be given if the project is late by five days. Prior to demonstrating your bonus project you must demonstrate and submit your basic one first.