

# ECE 4500/5540 DIGITAL ELECTRONICS

FALL 2011

## Project Assignment #1

(Team Project)

Total: 40 pts. (10% of course grade)

Due 3:00pm, Friday, November 4, 2011

Demonstrations in the B-214 Lab

### Specifications:

You are to develop a concise layout of a module that implements a simple **4-bit Arithmetic Logic Unit (ALU)**. The function chart of the ALU is given below. Assume **signed (two's complement)** number representation for the two operands **A** and **B**. The data inputs are as follows **A3-A0**, **B3-B0** (A3 and B3 being the most significant bits, respectively), **CIN** (Carry In), and **CC2-CC0** (Command Code bits, CC2 is most significant). The outputs are as follows: **F** (Function) outputs **F3-F0** (F3 being the most significant bit), **COUT** (Carry Out), **S** (Sign), **Z** (Zero), and **OVF** (Overflow). You can study various complex combinational logic architectures by reading a few sections of Chapter 11 of the Text. In addition, you can review an ALU and Function Generator chip by Texas Instruments under part number SN74AS181.

#### Command Code CC

CC2 CC1 CC0

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1 1 0

1 1 1

#### Function F

A

NOT(A)

A AND B

A OR B

A XOR B

A PLUS B w/o Carry (CIN = 0)

A MINUS B w/o Borrow (no initial Borrow)

B

The two **arithmetic** operations affect **all** flag outputs (you **don't** need to implement any flag register bits at this time, though). For the **four logic** operations **OVF must be set to 0**, **S** and **Z must** evaluate with respect to the two operands and the **status** of **COUT** is irrelevant. The two **move** operations **must** have the same effects on the flags than that of the logic operations. You can choose **any** design style for CMOS logic. Only **non-complemented** input signals are available. The terminal configuration of the layout should allow access to all input signals from the top, and all output signals from the bottom of the cell. The power lines should be on first-layer metal rails that pass completely through the cell in a horizontal direction.

Be as generous as you can with the widths of the power lines so that their current-carrying capabilities will be reasonably high. Use W/L ratios for your transistors such that the circuit outputs will exhibit near minimum average propagation delays. You are going to

work with a 0.25-micron CMOS technology, however, the minimum feature size ( $L_{\text{MIN}}$ ) should not be less than 1.2  $\mu\text{m}$  and  $W_{\text{MIN}}$  is 2.0  $\mu\text{m}$ .

### Tasks:

1. Give a **discussion** of the **main points** of your design.
2. Develop a **transistor-level schematics** for each symbol using **Design Architect**. Turn in a hard copy of the symbol-level **schematic diagram** of your circuit. In addition, give the **total transistor count**.
3. **Verify the correct operation** of your circuit using **Eldo and Zelga**. You should also obtain the **VTC** for **one F** output bit of your choice, as well as the **worst case  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$**  delay times for the **whole** circuit, and the average delay  $t_p$ . Plot your **simulation results** and **comment** on them.
4. **Design a layout** for your circuit using **Icstation**. Give the **size of area** of a rectangle that confines your design. Turn in a hard copy of the **layout diagram**.
5. Perform the **Parasitic Extraction of the layout using Calibre xRC**.
6. Give the **product** of the **area**,  $t_{\text{PLH}}$ , and  $t_{\text{PHL}}$ .
7. **Demonstrate** the working project to the Lab Instructor.

### Submissions:

**Project Report** (hard copy) that includes:

- a) Introduction
- b) Discussion of your design
- c) Transistor-level schematic diagrams and symbol-level schematics for the whole module
- d) Simulation timing diagrams along with comments
- e) Final specs of your circuit (size of area, and area-delays product included)
- f) Printout of the Mentor layout
- g) Conclusions

Each Team must submit a **joint** Project Report.

**Bonus credit:** the **best** design (chosen in terms of the **minimum product** of the layout area and the two post-layout propagation delay values) will be given up to **+2% extra credit** at the discretion of the course instructor.

**Note:** you will lose 4 pts. by each day your project is tardy. **No** credit will be given if the project is late by five days.

Please pay close attention to the **narrative section** of your Project Report. Too short, non-informative narratives will result in loss of credit for the project.