

# ECE 4500/5540 DIGITAL ELECTRONICS

FALL 2011

ECE 4500 Bonus Project Assignment #2

ECE 5540 Bonus Project Assignment #3

(Team Project)

Total: 16 pts. (4% of course grade)

Due 2:00pm, Thursday, December 8, 2011

Demonstrations in the B-214 Lab

## Specifications:

The architecture for this Bonus Project is outlined on Page 3. It represents the ALU and the associated Dual Register Banks (referred to as **RALU**) of a simple, three-address, 4-bit RISC processor. To create that you are to link the modules you have developed for Projects #1 and #2 (ECE 4500 Section), or #3 (ECE 5540 Section) and yet to add four **flag flip-flops CY, Z, S, and OVF**, along with **temporary register TMP2** and a set of **Three-State Buffers**. In order to establish a time base for the various control actions you are to introduce a **clock signal CK**. Use **Design Architect** and **Eldo** along with **Zelga** for functional design and simulation of your design, respectively. Then you should lay out the RALU using **IcStation**. You are going to work with a 0.25-micron CMOS technology, however, the minimum feature size ( $L_{MIN}$ ) should not be less than 1.2  $\mu\text{m}$ .

## Tasks:

1. Give a complete **discussion** of your design. Your **focus** should be on the **new modules** and the **links** between the modules rather than the ones that have been already documented in Projects #1 and #2 (ECE 4500), or #3 (ECE 5540). That includes the sizing of the transistors.
2. Plot a transistor-level **schematic diagram** for each of your **new circuit modules (symbols)**.
3. Obtain a **functional simulation** of your RALU using Eldo and Zelga. The algorithm is as follows: the first step of a functional test should involve loading data into selected registers (source operands) of the two register banks. Then some arithmetic or logic operation should follow in step two for which the source operands should be loaded into the two temporary registers TMP0 and TMP1, and contents of TEMP0 are routed to the A\_BUS and contents of TEMP1 are routed to the B\_BUS. The result of the operation is calculated by the ALU, and should be stored in TMP2. In addition, the flags should be properly set. In the third step the contents of TMP2 should be written into a destination register in any of the two register banks through the C\_BUS. Plot your simulation results and **comment on** them.  
Next, repeat these steps such that TEMP0 is now routed to the B\_BUS and TEMP1 to the A\_BUS.  
Determine the **maximum clock frequency** if steps 2 and 3 above were to be done in just one clock period, respectively.
4. **Lay out** each **new** functional circuit module, and the **whole** RALU unit. Print

out the **layout diagrams**. Give the **size** of the **layout area** for each new module, and the whole chip.

5. **Demonstrate** the working project to the Lab Instructor.

**Submissions:**

**Project Report** (hard copy) that includes:

- a) Introduction
- b) Discussion of your design
- c) Transistor-level schematic diagrams
- d) Simulation timing diagrams along with comments
- e) Final specs of your circuit (size of area included)
- f) Printout of the layout diagrams
- g) Conclusions

Each Team is to submit a **joint** Bonus Project #2, or #3 Report that is **separate** from the standard Project #2, or #3 Report.

**Note:** you will lose 2 pts. by each day your project is tardy. **No** credit will be given if the project is submitted **after** 5:00pm, Monday, December 12, 2011.