

ECE 4500/5540 DIGITAL ELECTRONICS

FALL 2011

ECE 4500 Project Assignment #2

ECE 5540 Project Assignment #3

(Team Project)

Total: 40 pts. (10% of course grade)

Due 2:00pm, Thursday, December 8, 2011

Demonstrations in the B-214 lab

Specifications:

Design a **Dual 4 × 4-Bit Register Bank (DRB)** by using any design style in **static CMOS** technology. Each bank of the DRB (Registers **R0 - R3**, and **R4 - R7**, respectively) should include the necessary address decoder, read/write, pre-charge, sense amplifier, temporary buffer register and three-state buffer circuits. Please refer to Page 3 for the basic architecture, and to the “Hints” (five pages) that are posted under the Design Clinic Section of the Class Web Page. The DRB is specified such that one bank may be accessed simultaneously with the other one. However, **no more than one set** of TS Buffers can be in low-impedance state on the **A_BUS** and **B_BUS**, respectively. Your final design should only have the following input and output signals:

- **B0_S**, and **B1_S** active-high Bank Select signals,
- **B0_DIN0 - 3**, and **B1_DIN0 - 3** data input lines,
- **B0_A0 - A1**, and **B1_A0 - A1** address lines, where A1 is most significant,
- **B0_R/W***, and **B1_R/W*** Bank Read/Write* signals (sign * stands for active low signal),
- **B0_LD**, and **B1_LD** signals (active-high) to load temporary registers **TMP0** and **TMP1**, respectively,
- **EN0_A**, **EN0_B**, **EN1_A**, and **EN1_B** TS buffer enable signals (active-high),
- **A_BUS0 - 3**, and **B_BUS0 - 3** data output lines,
- **VDD** and **VSS**.

The terminal configuration of the layout should allow access to all input signals from the top, and all output signals from the bottom of the cell. The power lines should be on first-layer metal rails that pass completely through the cell in a horizontal direction.

Be as generous as you can with the widths of the power lines so that their current-carrying capabilities will be reasonably high. Use W/L ratios for your transistors such that the circuit outputs will exhibit near minimum average propagation delays. You are going to work with a 0.25-micron CMOS technology, however, the minimum feature size (L_{MIN}) should not be less than 1.2 μm .

Tasks:

1. Give a complete **discussion** of your design that includes all internal modules and sizing of the devices.

2. Develop **transistor-level schematic diagrams** for each **circuit modules (symbols)** and the **SRAM cell** using **Design Architect**. Turn in a **hard copy** of the schematics for each symbol and the top-level module. In addition, give the **total transistor count**.
3. **Verify the correct operation** of your circuit using **Eldo and Zelga**. Plot your **simulation results** and **comment** on them.
The **functional simulations** should cover **both banks**. The tests should include **writing** data **0xA** followed by **two back-to-back read** operations at **locations R1**, and **R3** (as well as **R5 and R7**), respectively. The output data should be verified at the **A_BUS** and **B_BUS** data lines, respectively. In addition, use **Eldo and Zelga** to obtain V_{OL} and V_{OH} for data lines **A_BUS0** and **B_BUS3**, respectively (refer to Page 3 of the Hints), as well as **min. read access** and **cycle times**, respectively, with respect to the **rising edge of the B0_S signal**. You should also obtain the **min. write cycle time** for bit **Q1 of Bank #1** (again, refer to Pages 3 and 5 of the Hints), the **min. pulse width of the B1_R/W*** signal, and the **min. data setup time** with respect to the **rising edge of the B1_R/W* signal**. Plot your simulation results and **comment** on them.
4. **Design a layout** for your circuit using **Icstation**. Give the **size of the layout area** of each symbol and the whole design. Turn in a hard copy of the **layout diagram** of the **DRB**.
5. Perform the **Parasitic Extraction of the DRB layout using Calibre xRC**.
6. **Demonstrate** the working project to the Lab Instructor.

Project Report (hard copy) that includes:

- a) Introduction
- b) Discussion of your design
- c) Transistor-level schematic diagrams
- d) Simulation timing diagrams along with comments
- e) Final specs of your circuit (size of area, and area - access time delays product included)
- f) Printout of the layout diagram
- g) Conclusions

Each Team must submit a **joint** Project Report.

Bonus credit: the best design (chosen in terms of the **minimum product** of the layout area and the read and write access time delays) will be given up to **+2% extra credit** at the discretion of the course instructor.

Note: you will lose 4 pts. by each day your project is tardy. **No** credit will be given if the project is submitted **after** 5:00pm, Monday, December 12, 2011.