

ECE 4500/ECE 5540 DIGITAL ELECTRONICS
FALL 2011
Syllabus

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Hours: MW 4:30-5:20pm, or by appointment
Class: MWF 3:30-4:20pm, Room C-124, CEAS
Lab: R 6:30-9:20pm, Room B-214, Microcontrollers Lab, CEAS
Lab TA: Mr. Sai Guruva Avuthu
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Hours: posted on the Class Web Page

Course Objective

The purpose of this course is to develop techniques for analyzing and designing digital integrated circuits. For logic circuit implementations, the CMOS technology will be considered. The course will start with a brief review of the state-of-the-art technology, followed by fundamental models of CMOS transistors. Next, a detailed description and analysis of the core digital design block, being the inverter, will be given. It will be followed by the design of more complex logic gates, such as NAND, NOR, and XOR, looking at optimizing the speed, area, or power. The learned techniques will be applied on MSI level building blocks, such as adders and multiplexers. Substantial attention will be devoted to the discussion of sequential circuits, clocking approaches, and memories. The course will be concluded with the discussion of the impact of interconnect parasitics on the design performance and approaches to cope with them. Significant emphasis will be placed on the use of CAD Tools (Mentor Graphics Electronic Design Automation tools) for labs, homework assignments, and projects.

Materials Used in Class

1. Text: *Digital Integrated Circuits* by Jan M. Rabaey, Second Edition, Prentice-Hall, 2003, available in the University Bookstore, Bernhard Center, required
2. Materials disseminated using the ECE 4500 Class Web Page (official media for the class), required
3. Richard C. Jaeger, *Microelectronic Circuit Design*, available at the Reserve Desk of Waldo Library as a reference

Prerequisites: ECE 2210, ECE 2500, and ECE 3570, or graduate standing

Exams, Homework, and Projects

There will be one midterm exam, and a two-hour final exam. The dates of the in-class exams are as follows: **3:30 - 4:20pm, on Friday, October 14, 2011 (Midterm)**, and **12:20 - 2:30pm, on Monday, December 12, 2011 (Final Exam)**. Exams will consist entirely of design-oriented problems. The Final Exam will be comprehensive over all course material, however, more weight will be allocated to topics subsequent to the Midterm Exam. Students are required to attend all exams as scheduled, failure to do so

will result in a zero score for any examination not attended (if an emergency arises, you must contact the course instructor before any examination).

Design-oriented homework problems will be assigned to improve students' problem-solving skills, and to prepare the students for the lab experiments and tests. **Homework is an individual assignment!** Solutions must be done in a structural, logical, and orderly manner with frequent brief notations enabling the grader to readily verify your sources of information, steps taken, sources of formulae and equations, and methods used. About half of the homework assignments will require the use of the Mentor Graphics software in the lab. **No late homework** will be accepted.

Two Team Design Projects will be assigned in the **undergraduate section** to prepare the students to work in a team of designers. **An additional project (three projects total)** will be given to the **graduate students**. Late projects will be penalized by losing 10% of credit for each day the project is tardy, however, no credit will be given after five days. No projects will be accepted after the last day of classes. The Project Team assignments will be made by the course instructor in a random fashion and will be posted on the Class Web Page. If you had a concern regarding to the effort of your project team partner you should talk to the course instructor in a timely manner before the project is due.

Lab Work

It will include **nine experiments**, two of which will be of two-session ones. A **Lab Final Exam** will conclude the lab **6:30-9:20pm, on Thursday, December 8, 2011**. A **detailed lab session outline** is posted on the Class Web Page, however, some of the main points are also summarized here. Work on the experiments will be done in teams of two students. The Lab Team assignments will be made by the course instructor in a random fashion and will also be posted on the Web. If you had a concern regarding the effort of your lab team partner you should talk to the course instructor. Most laboratory experiments will require prelab work in the form of written calculations, or developing a computer file for modeling and simulation of a circuit. Extensive use of the Mentor Graphics EDA tools such as Design Manager, Design Architect, Eldo Simulator, Xelga Viewer, Icstation, and Calibre Xrc will be required. The **Linux-versions** of these programs will be running on **PC Workstations** in the **B-214 Microcontrollers Lab**. The **Lab Guidelines** and the **Mentor Tutorial** that are posted on the class Web Page cover for the necessary steps to launch and use the Mentor tools, however, **students are responsible to familiarize with the software at their own**. In the lab students **must** demonstrate the **DRC check** and the **LVS check** of their circuits to the Lab TA along with **appropriate simulation results**. In addition, **hard copy Lab Reports** will be also required.

If you don't show up for a lab, you forfeit the points associated with the entire lab that week, and cannot later make up the lab. Exceptions will be made only for those individuals who contact the Lab TA before the lab, giving an adequate reason why they cannot attend that day. **Note: you must achieve a passing grade in the lab (total 60% out of 100%) in order to pass the class.**

Grading

Grades will be determined on the basis of performance on exams, projects, labs, and homework, according to the following weights:

ECE 4500 Section		ECE 5540 Section	
Homework	10%	Homework	10%
Midterm Exam	20%	Midterm Exam	15%
Project #1	10%	Project #1	10%
Project #2	10%	Project #2	10%
Lab Work	20%	Project #3	10%
Final Exam	30%	Lab Work	20%
		Final Exam	25%

A:	83 - 100%
BA:	78 - 82%
B:	69 - 77%
CB:	63 - 67%
C:	53 - 62%
D:	43 - 52%
E:	<43%

In borderline cases, the Final Exam may be given a higher weight, at the instructor's discretion.

Project Dates, ECE 4500 Section

Project 1 due: 5:00pm, on Friday, November 4, 2011

Project 2 due: 2:00pm, Thursday, December 8, 2011

Demonstrations will be given in the B-214 Lab

Project Dates, ECE 5540 Section

Project 1 due: 5:00pm, on Friday, November 4, 2011

Project 2 due: 3:00pm, Friday, November 18, 2011

Project 3 due: 2:00pm, Thursday, December 8, 2011

Demonstrations will be given in the B-214 Lab

Exam Dates

Midterm Exam: 3:30 - 4:20pm, on Friday, October 14, 2011, Room C-124

Lab Final Exam: 6:30-9:20pm, on Thursday, December 8, 2011, B-214 Lab

Final Exam: 12:30 -2:30pm, on Monday, December 12, 2011, Room C-124

Codes, Policies, Processes and Procedures

The ECE 4500/5540 Web Home Page will be used as official communications media for the class. Students must check the Home Page for new information and/or assignment revisions on a daily basis.

The WMU College of Engineering and Applied Sciences Honesty Code will apply in this course.

You are responsible for making yourself aware of and understanding the policies and procedures in the Undergraduate Catalog or the Graduate Catalog, respectively, that pertain to Academic Integrity. These policies include cheating, fabrication, falsification and forgery, multiple submission, plagiarism, complicity and computer misuse. If there is reason to believe you have been involved in academic dishonesty, you will be referred to the Office of Student Conduct. You will be given the opportunity to review the charge(s). If you believe you are not responsible, you will have the opportunity for a hearing. You should consult with the course instructor if you are uncertain about an issue of academic honesty prior to the submission of an assignment or test.

Homework is individual work. Students may discuss with their classmates the basic approaches to arrive at the solutions **in principle**. However, they are not allowed to share circuit schematics, calculations, Mentor Graphics files, and the like. Similarly, there **must not be leaks of concrete design information** across lab teams and project teams, respectively.