

ECE 5540 DIGITAL ELECTRONICS

FALL 2011

Project Assignment #2

(Team Project)

Total: 40 pts. (10% of course grade)

Due 3:00pm, Friday, November 18, 2011

Demonstrations in the B-214 Lab

Specifications:

You are to develop a concise layout of a module that implements a **Carry-Save Multiplier (CSMUL)** for **4-bit signed binary operands**. For ideas you can study the relevant sections of Chapter 11 of the Text. The data inputs are as follows **A3-A0, B3-B0** (A3 and B3 being the most significant bits, respectively). The outputs are **Z7-Z0** (Z7 being the most significant bit). The two inputs are assumed to be in 2's complement representation, the product output should be generated in 2's complement form as well.

You can choose **any** design style for CMOS logic. Only **non-complemented** input signals are available. The terminal configuration of the layout should allow access to all input signals at two sides of the cell, and all output signals at the other two sides of the cell. The power lines should be on first-layer metal rails that pass completely through the cell in a horizontal direction.

Be as generous as you can with the widths of the power lines so that their current-carrying capabilities will be reasonably high. Use W/L ratios for your transistors such that the circuit outputs will exhibit near minimum average propagation delays. You are going to work with a 0.25-micron CMOS technology, however, the minimum feature size (L_{MIN}) should not be less than 1.2 μm and W_{MIN} is 2.0 μm .

Tasks:

1. Give a **discussion** of the **main points** of your design. It should include your algorithm and a block diagram of the signed multiplier.
2. Develop a **transistor-level schematics** for each symbol using **Design Architect**. Turn in a hard copy of the symbol-level **schematic diagram** of your circuit. In addition, give the **total transistor count**.
3. **Verify the correct operation** of your circuit using **Eldo and Zelga**. You should also obtain the **VTC** for **one Z** output bit of your choice, as well as the **worst case t_{PLH}** and **t_{PHL}** delay times for the **whole** circuit, and the average delay **t_p** . Plot your **simulation results** and **comment** on them.
4. **Design a layout** for your circuit using **Icstation**. Give the **size of area** of a rectangle that confines your design. Turn in a hard copy of the **layout diagram**.
5. Perform the **Parasitic Extraction of the layout using Calibre xRC**.
6. Give the **product** of the **area**, **t_{PLH}** , and **t_{PHL}** .
7. **Demonstrate** the working project to the Lab Instructor.

Submissions:

Project Report (hard copy) that includes:

- a) Introduction
- b) Discussion of your design
- c) Transistor-level schematic diagrams and symbol-level schematics for the whole module
- d) Simulation timing diagrams along with comments
- e) Final specs of your circuit (size of area, and area-delays product included)
- f) Printout of the Mentor layout
- g) Conclusions

Each Team must submit a **joint** Project Report.

Bonus credit: The best project (the product of the circuit area and the two propagation delays is at minimum and a complete report in good quality) may earn up to **2% extra credit** at the discretion of the course instructor.

Note: you will lose 4 pts. by each day your project is tardy. **No** credit will be given if the project is late by five days.