

P3

(4)

a) The worst case input combination wrt keeping  $V_{OL}$  as low as possible (with a given  $(\frac{W}{L})_{PMOS}$ ) is when 3 NMOS devices with the smallest  $W/L$  are ON, in series.

ABCD = 1110 . Bigger Req<sub>n</sub>  $\rightarrow$  smaller  $(\frac{W}{L})_{PDN}$

$$V_{OL} = \frac{k_p (V_{DD} + V_{TP}) \cdot V_{DSATP}}{k_n (V_{DD} - V_{TN})}$$

$$k_n = k_n' \left(\frac{W}{L}\right)_{PDN}$$

$\uparrow$  smaller  $(\frac{W}{L})_{PDN}$  yields bigger  $V_{OL}$

$$b) \left(\frac{W}{L}\right)_{PDN} = \frac{1}{\frac{1}{8} + \frac{1}{6} + \frac{1.2}{2.0}} = \frac{1}{\frac{13}{24} + \frac{4}{24} + \frac{14.4}{24}} \approx 1.121$$

$$0.15 \geq \frac{\cancel{30 \cdot 10^{-6}} \cdot \left(\frac{W}{L}\right)_p \cdot (2.5 + (-0.4)) \cdot (-1)}{115 \cdot \cancel{10^{-6}} \cdot 1.121 \cdot (2.5 - 0.43)}$$

$$\underline{\left(\frac{W}{L}\right)_p} \leq \underline{0.635}$$

Considering the constraints imposed by the MIT Design Kit, a possible choice is

$$\underline{W = 2.0 \mu\text{m} \text{ and } L = 3.2 \mu\text{m}}$$

that corresponds to  $\left(\frac{W}{L}\right)_p = 0.625$