

ECE 4500/5540 DIGITAL ELECTRONICS

Fall 2011 Laboratory Session Outline

Lab Instructor: Mr. Sai Guruva Avuthu

Meeting times: R 6:30pm – 9:20pm in Laboratory B-214

Office hours: will be posted on the Class Home Page

Email: saiguruva.r.avuthu@wmich.edu

Lab Assignments: have been posted on the Class Home Page

Pre-lab Assignments: will be posted on the Class Home Page

Lab Work

The lab will cover nine experiments, with two of them being two-session labs. Lab work will be done in teams of two students to develop skills for collaboration. However, the course instructor may assign three students or just one student to a team. Team assignments will be decided by the course instructor and will be posted on the Class Web Page. Starting with Lab 2, students are required to complete a pre-lab assignment. This will enable students to make full use of the available lab time. Students are also expected to take advantage of the extended lab hours in the B-214 Lab.

Students will be using the Mentor Graphics EDA tools. These tools run under Red Hat Linux. **At the end of each lab session students must save all their work on their thumb-drives and are required to delete the files from their work folders on the hard drives in the B-214 Lab.** This is to prevent even accidental plagiarism in the lab. Teams are required to submit a hard copy lab report for each lab (**but for Lab 1**) to the Lab TA. Lab Reports are due **on the day before the next lab at 5:00pm**, i.e., at **5:00pm on Wednesday**, in the office of Mr. Sai Avuthu (Room B-214, Microcontrollers Lab). **Late submissions will be penalized by 15% credit per day** the report is tardy. Reports will **NOT** be accepted **after 3 days of the due date**.

Before a new lab starts (Lab 3 to Lab 9), students are required to run the **DRC check** and the **LVS checks** on both the overall design and the cell level design, respectively, **of the prior lab** and show them to the Lab TA. The TA will review the full designs to make sure that the teams have actually completed the previous lab before starting a new one. After the verification of the results of the prior lab is done students will present their pre-labs to the Lab TA.

If you do not show up for a lab, you will not be given any points for that lab. There will be **no** make up labs. Exceptions will be only made for students who have provided adequate reasons, and who have given a notice at least a day in advance to the Lab TA that they cannot attend the lab that day. Students have to achieve **a passing grade in the lab (60% out of 100%)** in order to pass the class.

Starting with Lab 3, bonus credits may be given to one team who produce a complete and high-quality lab report along with the most efficient design (details will be given by the Lab TA). Decisions on the bonus credits will be made by considering the **product of the layout size** and the **two propagation delays** (should be at minimum), as well as the **quality of the simulation results** for the assigned design. Bonus credits may not be given to any team if all requirements are not met.

The **Lab Final Exam** will be given **6:30-9:20pm, on Thursday, December 8, 2011**. The time frame will be split into two sessions. In each session a different test problem will be assigned.

Students will have about 1 hour and 20 minutes to complete the test. Sign-up sheets for the Lab Final sessions will be posted approx. one week before the lab final.

Grading

Lab work: 20% of the course grade

Each lab (Labs 2 to 9): 13 points, out of which is up to 3 points for the pre-lab assignment (104 points total)

Lab Final: 39 points

Lab bonuses (Labs 3 to 9): 12 points max. (2 points max. per lab)

Note: Grades will be posted weekly on the Class Web Site.

Report format

(No hand written work except comments on simulation results)

1. Front cover
2. Lab description and design approach (not more than 1 page)
3. Schematic Design (Circuit diagram – Design Architect)
4. Eldo Simulations/Xelga Viewer – Pre-layout timing diagrams
 - Suitable input stimuli
 - DC Sweep (if needed)
 - Propagation delays (t_{plh} and t_{phl})
 - Performance calculations (based upon the t_{plh} and t_{phl} values obtained via simulation)
5. IC Layout – Layout Graphics
6. LVS report (important!)
7. Calibre-based Post Layout DRC checks
8. Calibre-based Post Layout LVS report (upper level cell check necessary)
9. Parasitic extraction of the IC vs. Schematic Diagram
9. Conclusion
 - Transistor count
 - IC layout size
 - Propagation delays (t_{phl} and t_{plh})
 - Product of the layout size and the propagation delays (the potential extra credit will be primarily given on the grounds of this value).

Lab report score break up (may change based upon the assigned tasks)

Schematic design: 10%

Eldo simulations (pre-layout): 40%

IC Layout: 40%

Calibre reports (assuming IC level is correct): 10%

Honesty Code

The ECE 4500/5540 Web Home Page will be used as official communications media for the class. Students must check the Home Page on a daily basis.

The WMU College of Engineering and Applied Sciences Honesty Code will apply in this course.

You are responsible for making yourself aware of and understanding the policies and procedures in the Undergraduate Catalog and in the Graduate Catalog, respectively, that pertain to Academic

Integrity. These policies include cheating, fabrication, falsification and forgery, multiple submission, plagiarism, complicity and computer misuse. If there is reason to believe you have been involved in academic dishonesty, you will be referred to the Office of Student Conduct. You will be given the opportunity to review the charge(s). If you believe you are not responsible, you will have the opportunity for a hearing. You should consult with the Lab TA and/or the course instructor if you are uncertain about an issue of academic honesty prior to the submission of an assignment or test.