

ECE 4500 Digital Electronics Required Course

2007-2008 Catalog Data: ECE 4500: Digital Electronics
The electrical and logic aspects of digital integrated circuits and their applications.
Credit: 4 hours
Prerequisites: ECE 2210, ECE 2500, ECE 3570

Textbook(s) and/or Required Materials: 1. Jan M. Rabaey, *Digital Integrated Circuits, A Design Perspective*, Second Edition, Prentice Hall, 2003

2. Materials disseminated using the [ECE 4500 Class Web Page](#) (the official media for the class). They include tutorials on how to work with Mentor Graphics IC Nanometer Technology tools.

Recommended Materials: Instructor's Lecture Notes

References: Richard M. Jaeger, *Microelectronic Circuit Design*, McGraw Hill, 1997

Coordinator: Dr. Janos L. Grantner, Professor, ECE

Instructor in the Spring 2008 Semester: Dr. Janos L. Grantner

Prerequisites by topic:

1. Basic knowledge of device physics
2. MOS transistor circuit operation
3. Digital logic design
4. Basic knowledge of UNIX

Course Objectives: (ABET Learning Outcomes)

This course develops

1. To provide experience to model, analyze, design and simulate digital integrated circuits (a, b, c, e).
2. To provide experience to work with Mentor Graphics IC Flow tools (k).
3. To provide experience to choose a suitable circuit design style to meet the required specs (c).
4. To develop skills to prepare effective written technical communications for engineering analysis and design work through project reports (g).
5. To assess the students' knowledge of contemporary issues (j).
7. To assess the students' skills to use modern tools of engineering practice (k).

Topics:

1. Course overview, the state-of-the-art of microelectronics design and nanotechnology (2 classes)
2. MOSFET transistor models, static and dynamic behavior (3 classes)
3. The static CMOS inverter: static and dynamic behavior, power consumption, the effects of technology scaling (4 classes)
4. Design of combinational logic gates in CMOS: static and dynamic design styles, power consumption (9 classes)
5. Design of sequential logic circuits: static and dynamic sequential circuits, non-bistable sequential circuits (10 classes)
6. Design of memory and array structures: the memory core, memory peripheral circuits (6 classes)
7. Timing issues in digital circuits (4 classes)
8. Coping with interconnect (4 classes)
9. Test (1 class)

Course/Laboratory Schedule: 3 one-hour lectures, one 3-hour laboratory

Laboratory Experiments:

1. Familiarization with the Mentor Graphics IC Nanometer Technology tools (2 sessions)
2. Design, Simulation and Layout Editing of a Static Complementary CMOS gate (1 session)
3. Design of a Two-Input XOR Gate Using Pass Transistor Logic (1 session)
4. Design of a One-Bit Full Adder Module (2 sessions)
5. Design of a One –of-Four Multiplexer Module Using Dynamic Logic (1 session)
6. Design of a Static SR Flip-Flop (1 session)
7. Design of a Two-Bit Synchronous Counter (1 session)
8. Design of a 4 bit \times 1 Bit Section of a Static 4 Bit \times 4 Bit Register Bank (2 sessions)
9. Design of a Muller C-Element (1 session)
10. Lab Final (1 session)

Design Projects:

1. Design of 4-bit parallel ALU (a bonus project is also offered, 4 weeks). A report is required.
2. Design of a Dual 4x4 Bit Register Bank (a bonus project is also offered, 4 weeks). A report is required.

Evaluation:

1. Examinations (50%)
2. Lab work (20%)
3. Design Projects (20%)
4. Homework (10%)

Computer Usage:

Mentor Graphics IC Nanometer Technology tools are used to carry out the design, simulation and layout editing tasks for labs, projects and most of the homework assignments.

Contribution to Professional Component:

ABET professional component content as estimated by faculty member who prepared this course description:

Engineering sciences:	2 credits or 50%
Engineering design:	2 credits or 50%

Relation of Course to Program Outcomes:

This course provides significant support for the CE program objectives Depth and Professionalism along with learning outcomes: a, b, c, e, g, j, and k.

Prepared by: Dr. Janos L. Grantner

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