

INFORMATION FOR THE LAB FINAL

For the Lab Final, you are allowed to bring in any **hard copy** reference material. That includes a hard copy of the Mentor Graphics Tutorial, the Text, copies of your **own** Lab Reports, Project Reports and Homework Assignments. However, you are **not** allowed to access to **any file** in your account, any project account, or any other account on the Web. Those who don't comply with this constraint will be receiving a **0 score** for the Lab Final. A **0 score** will also be given to students who talk to each other, or use any form of communication or messaging device/service during the Lab Final.

You will be required to create a schematic diagram for a given design problem (in the range of 6-12 transistors). The Final will primarily consist of **three** tasks as follows: **schematic design** (Design Architect), **pre-layout simulations** (Eldo and Zelga), and **IC layout design** (ICStation). Your design should pass the **DRC and LVS tests**. You will **demonstrate** the schematics, the simulations, and the outcome of the DRC and LVS tests, respectively, to the Lab TA. In addition, you will **turn in the Exam Sheet**, and **hard copies** of your **schematics**, the **simulation results**, and the **top page** of the **LVS report**. **If you don't turn in your Exam Sheet you will be given a 0 for the test.** The Lab TA may wave the requirement to print some of the hard copies referred to above.

This time the Lab TA will **not** help you in completing the assigned tasks, or answer any questions beyond the clarification of the test problem. Every step through the design process should have been familiarized by each student, by now.

A **Sign-up Sheet** has been posted in the B-214 Lab. **No more than 9 students** are allowed to sign up for a session. The lab final will take approximately **1 hour and 20 minutes**. Students who finish the test early will **not** be allowed to leave. All students will leave at once after the Lab TA has checked out all the demos and collected all the required hard copies. **Students who do not show up for the lab final will be given a 0 score.** Students who come late for the lab final will not be given extra time to complete it. Make up tests will only be given under extraordinary circumstances and only if the course instructor, or the lab instructor has been notified **prior to** the test.

Lab Final study guide: Complementary CMOS, pseudo NMOS, pass transistor logic, and dynamic CMOS logic.

General comments:

It is going to be a very straightforward Lab Final and it is not going to be something brand new that you have never worked on in the lab. It may be a little bit tricky but if you find yourself spending too much time on the design, then you obviously have not fully understood the labs throughout the semester. Just study the four design styles above and keep in mind that it is only 6-12 transistors so it can't be that hard after all.