ECE 5570 DESIGN OF RECONFIGURABLE DIGITAL MACHINES

FALL 2012

Homework Assignment #2

Total: 80 pts.

Due 4:30pm, Thursday, September 27, 2012

You are to develop **VHDL** code for a **chip** that is **functionally equivalent** to the **TI SN74AS869 Synchronous 8-Bit Up/Down Counter** circuit. Use the available **Xilinx and ModelSim tools to design, simulate and map** your circuit to a Xilinx **XC3S500E-FG320-5** FPGA chip. The **Data Sheets** for the SN74AS869 chip can be found on **Texas Instrument**'s Web Page (www.ti.com). You **don't** have to implement the **propagation delays** given in the Data Sheets.

a) Turn in a hard copy of the **.vhd** file for your design. (30 pts.)

b) Map your design to the XC3S500E-FG320-5 chip by running the **Implement** step. Use the User Constraints to create a **pin assignments of your choice**. Turn in your **.ucf** file and the **device utilization** and **pin assignment** sections, respectively, of the **Summary Report**. (10 pts.)

c) Develop a **script** (**.do file**) to verify the correct operation of your circuit. **At minimum**, your .do file should replicate the signal waveforms as shown on Page 7 of the Data Sheets. Run the **behavioral simulations**.
Turn in a hard copy of your **.do** file along with printouts of the **simulation waveforms**. **Comment** on the simulation results for full credit. (40 pts.)

Fall back position: turn in your **.vhd**, **.ucf** and **.do** files along with comments for partial credit if you couldn't compile your design due to some fatal error.