Design, simulate, build, and demonstrate the correct operation of the simple strobed I/O chip specified below. A functional block diagram is given on Page 2. Timing diagrams are given on Page 3. Use one Xilinx Spartan3E FPGA chip (the one that is mounted on your Xilinx Nexys 2 Board), as well as off-the-shelf ICs and other parts (as needed). Input signals are to be driven by micro switches, output signals are to be displayed by Bar-LED Units. Pay attention to the control of the bi-directional D7-D0 Data Bus of the I/O chip. You should not assume that the input signals to your I/O chip are properly synchronized with respect to the CLK signal. You must use the 50MHz CLK signal available on your Nexys 2 Board. You are to provide for your own Nexys 2 Board, a solderless Breadboard, a FX2 MIB Board to access to the signals on the Hirose connector and electronic parts, respectively.

Description of Operation

The microprocessor interface to the I/O chip is only enabled when the CS* (Chip Select, active-low) signal is at low level. If CS* is at high level then the D7,…, D0 data bus signals must be in high-impedance state. Signals WR* (write) and RD* (read) cannot be asserted simultaneously (they are mutually exclusive). Signal RDY* should be asserted when CS* and either WR* or RD* are asserted.

The data on the D7,…, D0 lines should be captured in the POUT_reg register at the ↑ edge of the WR* signal while CS*=0 and A1=A0=0. When generated, signal OUT* must have a pulse width of at least 60ns.

It is guaranteed that the minimum pulse with for signal INP* is at least 70ns. It is also guaranteed that the data on the P7,…, P0 peripheral data lines is stable when INP* is asserted. Signal INP* can be asserted at any point in time and the data on the PIN7,…, P0 lines should be captured in the PIN_reg register regardless of the status of the signals of the microprocessor interface.

Register bit INP_S* is set to low when the low level of signal INP* is sensed by the I/O chip and it is set back to high by the ↑ edge of the RD* signal while CS*=0 and A1=1 and A0=0.

When signal RESET* is asserted signal OUT* and register INP_S* should return to high level.

The source of the I/O chip’s CLK signal is the 50MHz clock available on the Nexys 2 Board.
The programmer’s model (the microprocessor interface) is as follows:

<table>
<thead>
<tr>
<th>CS*</th>
<th>A1A0</th>
<th>WR*</th>
<th>RD*</th>
<th>D7… D0</th>
<th>POUT_reg7…0</th>
<th>OUT*</th>
<th>INP*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Z….Z</td>
<td>no change</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>↑</td>
<td>1</td>
<td>data</td>
<td>D7….D0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>X…X1</td>
<td>no change</td>
<td>-ve pulse</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>PIN_reg7…0</td>
<td>no change</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X…X, INP_S*</td>
<td>no change</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>Z….Z</td>
<td>no change</td>
<td>1</td>
</tr>
</tbody>
</table>

The D7,..., D0 microprocessor data bus signals should be driven by switches SW7,..., SW0 on your Nexys 2 Board. The status of the D7,..., D0 signals should be displayed on LEDs LD7,..., LD0 on the Nexys 2 Board. Signals RESET*, CS*, A1, A0, WR*, RD* and PIN7,..., PIN0 should be generated by switches on your Breadboard. Signals WR*, RD* and INP* must be made bounce-free. Signal OUT* must be visualized on a logic analyzer. Signals POUT7,..., POUT0, PIN7,..., PIN0 and RDY* should be visualized using LEDs on your Breadboard.

In order to facilitate the testing and debugging of the project a **signal protocol along with the expected results** will be posted on the Class Web Page.

**Tasks**

a) Draw a detailed schematic diagram for the whole system. Clearly show the partitioning of the system into standard ICs, other parts, and the FPGA chip. (6 pts.)

b) Use the Xilinx ISE 14.1 and the currently available ModelSim PE student version by Mentor Graphics to develop the FPGA segment of the system. You should prove the correctness of your design by post-route simulations. Turn in the printouts of your design files (.vhd, and .do files, as well as sections of your Pad Report with the resource utilization and the device pinout diagram, respectively), and your simulation timing diagrams. Comment on your simulation results.

**Hint:** Force pin assignments for your signals through the User Constraints Utility so when you need to modify your VHDL design file then you can still keep the wiring to the Nexys 2 Board unchanged. (30 pts.)

c) Build the whole system using your Nexys 2 Board, FX2 MIB Board and Breadboard and demonstrate its correct operation to the course instructor. (24 pts.)
d) Submit a Project Report.

Each student should submit a **Project Report**. The project is not done until a complete report is submitted. The report should have the main sections as follows: **Introduction, Design, Design Evaluation**, and **Conclusion**. Your solutions to Tasks a) to c) should be represented in the report. **Demonstrations** will be given either in class, or in the Microcomputer Lab, **Room B-214**.

**Note**: you will lose **6 pts. by each day** your project (**a demonstrated circuit along with the report**) is tardy. **No** credit will be given if the project is late by **four business days**.