Design, simulate, build, and demonstrate the correct operation of a Single-Port, 2Kx8 bit SRAM Memory Module that is interfaced to the External Bus of the 8-bit RISC processor core of Project #2. The logical address space of the External Bus is 64KB (64Kx8Bit), unless it will be revised to be smaller. You need to revise your RISC processor design such that upon asserting the RST# signal the contents of the Program Counter (PC) will be set to 0xF800. In addition, the chip should assert an active-low RSTO# output signal. The base address for the memory block must be 0x8F00. The Memory Module should make use of a Block RAM unit of the XC3S500 FPGA chip in Single Port configuration. No parity bit is required. For details with respect to the signals of a Block RAM and the Xilinx Core Generator program please refer to the Xilinx Spartan-3 Generation FPGA User Guide. The demonstration of the correct operation of the integrated RISC processor and SRAM Memory Module system should be carried out by initializing the SRAM memory with a suitable program that will be executed by the RISC processor core. For observation, a revised Single-Step Logic module should also be implemented along with Bar-LEDs to visualize the signals of the External Bus.

A functional block diagram for the Memory Module is shown on Page 2. It includes the Single Step Logic. The earlier Single Step Logic Module that has been specified for Project #2 should be removed. The new Single Step Logic Module should have both manual and auto modes.

Map your Memory Module to the Xilinx XC3S500E FPGA chip (the one that is mounted on the Nexys 2 Board), as well as off-the-shelf ICs and other parts (as needed). Input signals are to be driven by micro switches, output signals are to be displayed by Bar-LED Units. You must use the 25MHz BCLK signal generated by the RISC processor core circuit for timing the External Bus cycles as the clock input to the Nexys 2 Board. You are to provide for your own solderless Breadboard, the necessary electronic parts, and two Nexys 2 Boards, respectively.

Tasks:
1. Draw a detailed block diagram and a schematic diagram, respectively, for the whole system. On the schematic diagram clearly show the partitioning of the system into standard ICs, other parts, and the FPGA chips. (14 pts.)

2. Give the state transition diagram for the Control Unit of the Memory Module. (4 pts.)
3. Give the **program code** that will be placed in the Memory Module and be executed by the RISC processor core along with comments with respect to the expected results and the signal flow on the External Bus. (14 pts.)

4. Use the available **Xilinx ISE Foundation and Core Generator tools** along with the **current ModelSim SE by Mentor Graphics** to develop the FPGA segment of the Memory Module. You should prove the correctness of your design by **post-route simulations**. Turn in the printouts of your design files (.vhd, .ucf and .do files), as well as the **resource utilization and device pinout sections**, respectively, of your **Summary Report** and your **simulation timing diagrams**. **Comment** on your simulation results. (34 pts.)

5. **Build the whole system** (the RISC processor from Project #2 is connected to the SRAM memory module) and **demonstrate** its correct operation to the course instructor. (34 pts.)

Each steam should submit a joint **Project Report**. The project is not done until a complete report is submitted. The report should have the main sections as follows: **Introduction**, **Design**, **Design Evaluation**, and **Conclusion**. Your solutions to Tasks 1) to 4) should be represented in the report. **Demonstrations** will be given in the Microcomputer Lab, **Room B-214**.

**Note:** you will lose 10 pts. by each day your project (a demonstrated circuit along with the report) is tardy. **No credits** will be given after 5:00pm, Friday, December 7, 2012.