**Course Description**

The objective of this course is to develop skills for designing complex digital systems and system-on-chip (SOC) applications. Students are expected to have a background in digital logic design, computer architecture and in microprocessor/microcontroller systems design. The three design projects will be based upon Field Programmable Gate Arrays (FPGAs). Students will be designing their circuits in VHDL using professional CAD tools by Xilinx and Mentor Graphics. The subject matter is considered in the required text, the instructor's lecture notes, and the recommended texts. Additional materials will be posted on the Class Home Page. The Data Sheets of those chips that will be referred to in the design projects can be found in the respective manufacturers' Web sites.

**Prerequisites by topic:**
- Digital Design
- Computer Architecture
- Microcontroller Applications

**Topics** to be covered in this course include:

1. Review of timing hazards of combinational logic circuits
2. Review of the design of synchronous and asynchronous sequential circuits
3. FPGA architectures, placement and routing
4. Digital system design for FPGAs using Xilinx and Mentor Graphics tools
5. Platform FPGAs, SOCs
6. Reconfigurable devices and systems
7. Reconfigurable computing applications
8. Dynamic reconfiguration and its applications
9. Hardware/software co-design

**Required Textbook/Materials**

2. Data sheets for selected FPGAs, FPGA Development Boards and other components. Students are expected to locate and download the needed information from either the vendor's Web site, or from an on-line library.
3. ECE 5570 Parts Kit, **required**. Students can place an order for their Kits by the help of the IEEE Student Branch, or can order the parts by themselves.
Most recent versions of the Xilinx WebPack (14.1) and the free ModelSim PE software that can be downloaded from the respective Web sites free of charge, required.

**Recommended Textbook/Materials**


**Course Procedure**

There will be homework assignments to work on, three significant design projects to be completed and a Final Exam to be taken. No late homework will be accepted. Homework is individual assignment! Projects will be carried on in teams of two students each, or may be worked on individually. Project operational demonstrations must be made to the instructor prior to handing in the written project reports. Project demonstrations and written reports have firm due dates for full credit. Projects will be accepted up to four business days after due date (not after the Final Exam, though) but will be penalized by the loss of 10% credit for each day late. Failure to successfully complete a project will result in a failing grade for the course. Plagiarism and/or the copying/duplication of another student’s homework, or another team's design or written reports will result in zero scores for the homework, or project, respectively, for all individuals involved. Failure to attend the Final Exam will result in an X grade for the course. A make-up final exam will only be given under extreme circumstances, and in any case, students should ask for the course instructor's permission prior to the test.

**Grading Policy**

Grades will be determined on the following basis:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Homework</td>
<td>10%</td>
</tr>
<tr>
<td>Project 1</td>
<td>15%</td>
</tr>
<tr>
<td>Project 2</td>
<td>25%</td>
</tr>
<tr>
<td>Project 3</td>
<td>25%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>25%</td>
</tr>
</tbody>
</table>

It is expected that the breakdown for letter grades will be as follows:

- **100-89 A**, **88-82 BA**, **81-75 B**, **74-68 CB**, **67-61 C**, **60-54 D**, **53 and below E**, missed project or final exam E, or X as appropriate. The boundaries between grades may be individually lowered at the instructor’s discretion. In borderline cases, the final exam may be given a higher weight, at the instructor’s discretion.

**Project Due Dates**

Project demonstrations will be performed prior to the project due date and time either in class, or in the Microcomputer Lab (Room B-214). Both the demonstrations and the written project reports will be due on:
Project 1  6:30pm, Tuesday, October 23, 2012
Project 2  6:30pm, Tuesday, November 13, 2012
Project 3  6:30pm, Tuesday, December 4, 2012

Permission to miss any due date may be granted by the instructor under extreme circumstances. If permission is desired, a request must be made before the due date and should include either a signed doctor's explanation or a written explanation signed by an appropriate WMU officer.

Final Exam Date  7:15-9:15pm, Tuesday, December 11, 2012, C-141 CEAS

Codes and Policies

The ECE 5570 Web Home Page will be used as official communications media for the class.

The WMU College of Engineering and Applied Sciences Honesty Code will apply in this course.

You are responsible for making yourself aware of and understanding the policies and procedures in the Graduate Catalog that pertain to Academic Honesty. These policies include cheating, fabrication, falsification and forgery, multiple submission, plagiarism, complicity and computer misuse. The instructor will give you guidance to avoid problems of this kind. If there is reason to believe you have been involved in academic dishonesty, you will be referred to the Office of Student Conduct. You will be given the opportunity to review the charge(s). If you believe you are not responsible, you will have the opportunity for a hearing. You should consult with the course instructor if you are uncertain about an issue of academic honesty prior to the submission of an assignment or test.