

ECE 6050 ADVANCED MICROPROCESSOR APPLICATIONS

SPRING 2012

Project Assignment #1

Rev. 1

Team Project

Total: 80 pts. (20% of course grade)

Due 6:30pm, Thursday, February 16, 2012

Design ports and associated control circuits for a board named VME64x_BIU that is interfaced to the External Bus of the Freescale MCF5407 ColdFire Processor. A functional block diagram of the board is given on the next page. The schematic diagram should include the following:

- Local Bus address, data, and control line buffers (using 3.3V Low Voltage Logic chips). Name the Local Bus signals LB_xx where xx is the normal MCF5407 signal name, e.g. LB_A31,...,LB_A08, etc. Name the internal signals before/after buffering BIU_xx.
- Address decoder, registers and control logic to select the device being accessed through the MCF5407 External Bus and control the flow of data.

Address Range (in hex)

Devices

6000 0000 – 60FF FFFF	Dual Port SDRAM (32-bit port, 16Mbytes)
7000 0000 – 700F FFFF	VME64x Bus Data (32-bit port)
7010 0000 – 701F FFFF	VME64x Bus Address Latch (32-bit port)
7020 0000 – 702F FFFF	Reserved (32-bit port)
8000 0000 – 800F FFFF	VME64x Bus Addr. Mod. Latch (6-bit port)
8010 0000 – 801F FFFF	VME64x Interrupt Request (either way, 8-bit port)
8020 0000 – 802F FFFF	VME64x Interrupt Status (8-bit port)
8030 0000 – 8037 FFFF	MCF IRQ1# Vector Register
8038 0000 – 803F FFFF	MCF IRQ7# Vector Register

- A synchronous state machine to deal with the timing issues of your design. You may assume that a 50MHz (50 % duty cycle) clock generator (asynchronous with respect to the MCF5407 External Bus Clock signal BCLKO) is available as a timing reference.
- Any glue logic should be implemented using the Xilinx Spartan 3E chip that is mounted on the Nexys 2 Spartan-3E FPGA Board.

In order to simplify your design the MCF 5407 External Bus interface is limited as follows:

- no bus arbitration signals
- only the IRQ1# signal is available for external interrupts
- no signals associated with the embedded peripheral modules, the DRAM Controller and the DMA Module included
- no internal TA# signal programming

You may assume that the MCF 5407 external bus clock rate is 25 MHz (the core clock rate is set to 150MHz through the PLL). You should utilize three available programmable chip enable signals (CS5# - CS7#) of the SIM (System Integration Module). You should give the contents of the relevant chip select and bus control registers for your approach. You should assume that the MCF 5407 CPU will access to the assigned memory spaces in normal mode. You may assume that the MCF 5407 External Bus Operates using 3.3V signals. The SDRAM and the VME64x ports should support dynamic bus sizing (i.e., byte, half-word, and word data), however, each data type is required to be properly aligned.

Design your TA# signal control logic such that your unit will respond to a MCF 5407 bus cycles with the minimum number of inserted wait states, depending upon the needs of the selected memory space. No critical timing analysis is required for this project.

Tasks:

1. **Develop a .do file** to simulate a suitable set of MCF 5407 bus cycles in order to verify the correct operation of your MCF 5407 bus interface design.
2. Use VHDL and the Xilinx ISE tools along with ModelSim by Mentor Graphics to **design, simulate and implement your MCF 5407 interface module**. Map the MCF 5407 interface signals such that a meaningful subset of them will be accessible through the Hirose connector of the Nexys 2 Development Board.
3. **Plot a schematic diagram** of your circuits. On the schematic, all nets must have labels and all devices must have distinct names- such as Uxx, where xx is a number, e.g., U00, etc.
4. **Demonstrate** the correct operation of you MCF 5407 interface module **by simulation**. Use real-time (**post-route**) simulations.
5. Turn in a **Project Report**. Your Project Report should include the main sections as follows: Introduction, Design, and Conclusion.

The Class Web Page has pointers to relevant Data Sheets and User's Manuals. Additional materials can be found on the Xilinx, Digilent and Freescale Home Pages, respectively, and on the other related manufacturers' Web Pages.