

# ECE 6050 ADVANCED MICROPROCESSOR APPLICATIONS

## SPRING 2012

### Project Assignment #2

Rev. 1

### Team Project

Total: 100 pts. (25% of course grade)

Due 6:30pm, Thursday, March 22, 2012

Design a **dual port, 16MB 32-bit SDRAM memory block along with its controller** (referred to as SDRAMC) such that one of the memory ports will be interfaced to the MCF 5407 External Bus. Your design **should seamlessly integrate with the circuits you have developed in Project #1**. In addition, develop a hardware emulator for the MCF 5407 External Bus along with **single-stepping capability** for debug and verification purposes using a Nexys 2 Board.

The other memory port will be interfaced to the VME64x Bus in Project #3. A functional block diagram for this project is given on the next page. The schematic diagram should include the following:

- the SDRAM memory block such that only one SDRAM chip is given in full detail
- a rectangular representing the Spartan-3E chip that implements the SDRAMC and other necessary circuits for the SDRAM block
- parts external to the Spartan-3E chip and the memory chips (if any)

**Micron MT48LC16M8A2TG-6A** chips are assigned to implement the SDRAM memory block. The dual port access to the SDRAM block should be implemented by using TS Transceivers and Buffers mapped to the Spartan-3E chip. The required refresh rate is 64ms for all 4096 rows, and automatic refresh cycles should be used for all SDRAM chips.

The core of the SDRAMC will be a synchronous state machine to deal with the timing issues of your design. You may assume that a 50MHz (50 % duty cycle) clock generator (asynchronous with respect to the MCF 5407 Bus Clock) is available as a timing reference.

For the MCF 5407 External Bus hardware emulator you should establish a 25MHz CLKIN signal. Use the Hirose connector on the Nexys 2 Board to implement a **suitable subset** of the bus signals. By analyzing the performance of your SDRAM memory unit you should make a decision with respect to the necessary number of wait states on the MCF 5407 Bus and assert the proper input of the wait state generator circuit for Project #1.

### Tasks:

1. Develop **VHDL programs** to emulate a suitable set of MCF 5407 bus cycles in order to verify the correct operation of your SDRAM memory module. Provide for single-step capability. **Implement** this MCF 5407 bus emulator using a Nexys 2 Board.

2. Use VHDL and the Xilinx ISE tools along with ModelSim by Mentor Graphics to **design, simulate and implement your dual port SDRAM memory module**. The whole memory module should be partially emulated by a set of DIP switches and bar LEDs, respectively, on the Nexys 2 Board. Map the MCF 5407 interface-related signals such that they will be accessible through the Hirose connector of the Nexys 2 Board.
3. **Plot a schematic diagram** of your circuits. On the schematic, all nets must have labels and all devices must have distinct names- such as Uxx, where xx is a number, e.g., U00, etc.
4. **Demonstrate** the correct operation of the **full configuration** of the combined MCF 5407 bus interface and dual port SDRAM memory module **by simulation**. Use real-time (**post-route**) simulations.
5. **Demonstrate** the correct operation of the **subset** of the combined MCF 5407 interface and dual port SDRAM memory module **by using two Nexys 2 Boards**.
6. Turn in a **Project Report**. Your Project Report should include the main sections as follows: Introduction, Design, and Conclusion.

The Class Web Page has pointers to relevant Data Sheets and User's Manuals. Additional materials can be found on the Xilinx, Micron, Digilent and Freescale Home Pages, respectively, and on the other related manufacturers' Web Pages.