

# ECE 6050 ADVANCED MICROPROCESSOR APPLICATIONS

Fall 2007

Team Project Assignment #3

Version A

**Total: 40 pts. (10% of course grade)**

**Due 6:30PM, Tuesday, December 4, 2007**

## Tasks:

1. Create a new design folder for your **VME Master Module**. Compile the file for the **SPARTAN 3** chip on your Nexys Board using the Mentor Graphics tools along with the Xilinx WebPack 9.2i tools, or an older version. A link to information on the Nexys Board has been posted on the ECE 3550 class Home Page. (10 pts.)
2. Carry out a **post-route simulation** of your circuit. **Print out** and **comment on** your **simulation results**, as well as attach sections of the Pad Report on the **utilized resources** and the chip **pinout diagram**. Turn in your **Project Report** that should include a narrative introduction, a design section with .vhd and .do files along with your commented simulation timing diagrams, and a conclusion section. (14 pts.)
3. Construct a test circuit using DIP-Switches and Bar-LED modules. The FPGA signals should be separated from the rest of the circuit by suitable buffers. Download your chip configuration file to the FPGA. Verify the operation of your circuit and **demonstrate** it to the course instructor. The VME documentation and your simulation timing diagrams in Task 1 will be used to verify the correct operation of your circuit. (16 pts.)

**Hints:** Create a user constraint (.ucf) file so you won't need to change your circuit wiring even if you have modified your code in preparing for the demonstration.