

ECE 6050 ADVANCED MICROPROCESSOR APPLICATIONS

SPRING 2012

Project Assignment #3

Rev. 1

Team Project

Total: 120 pts. (30% of course grade)

Due 6:30pm, Thursday, April 12, 2012

Design the MCF 5407 local bus to **VME64x Bus interface** that was left unspecified in Projects #1 and #2. You **need** to carry over **all** modules from your Project #1 and #2 designs. Some of them will likely need a revision to accommodate for the VME functions. Map your design to the **Spartan-3E** chip on the Nexys 2 Board. A functional block diagram for the Project #3 circuits is posted on the Class Web page. Assume that the VME64x Bus System Clock rate is **12.5 MHz**. The specs of the basic VME Bus needed for this project can be found in the Instructor's Lecture Notes. The features of the VME64x that will also apply to this project can be found at **the link VME Bus References** on the Class Web Page. The following **VME functional modules** should be implemented on the VME_BIU Board:

- **VME Master** (a **DTB bus request** is initiated by the MCF 5407 CPU from the Local Bus) **A32, D32 (aligned Quad Byte read and write cycles only)**. If the VME bus access is **not a match**, your VME Master module **will assert IRQ7#** for the local MPC563 CPU, and **will not** request the DTB bus ownership), **RWD Requestor** (may or may not monitor **all** of the BR0*- BR3* signals) **using BR2*** (a central Priority Arbiter is assumed), **D08 ROAK** (Release-on-Acknowledge) **Interrupter using IRQ4*** (an interrupt request can be generated by the MCF 5407 CPU from the Local Bus), **IACKOUT* Daisy-Chain Driver**, and **Interrupt Handler** for VME **IRQ3***. For DTB transfers some bits of the **Reserved Port** should be used to provide for **Geographical Addressing**. The VME Master **may hold on** to the DTB ownership for **only one data transfer**. **IRQ1#** on the MCF 5407 bus should be used to handle the **IRQ3*** VME bus interrupt.

- **VME Slave** (the Dual-Port SDRAM Module can be accessed by a VME Master), **Geographical Addressing, A32, D32 (aligned Quad Byte read and write cycles only)**, the VME Slave module will assert **BERR***, otherwise).

The **detailed specifications** include the following:

1. On the schematic diagram include VME64x bus address, data, and control line buffers. Name the internal signals before buffering VME_xx. Use Three-State Buffers, high-current Transceivers, and Open Collector buffer gates, as needed.

2. With respect to the address decoder and control logic to select the **Slave Module**: the **Slot Number is set to 13** along with **odd parity**. The address range is **0xB000 0000 – 0xB0FF FFFF**. **User and supervisor data and program** space, respectively, are assigned to this memory module. Signal **BERR*** should be asserted on the VME Bus if the data transfer request is **not** an aligned Quad-Byte.

3. On the schematic, all nets must have labels and all devices must have distinct names, e.g., Uxxx, etc.

Tasks:

1. Develop a set of **.do files** to simulate a suitable set of MCF 5407 and VME64x bus cycles in order to verify the correct operation of your VME Master and Slave functions.
2. Use VHDL and the Xilinx ISE tools along with ModelSim by Mentor Graphics to **design and simulate your complete VME_BIU module**. The whole memory module should be simulated by a set of macro commands in your .do file.
3. **Plot a schematic diagram** of your circuits. On the schematic, all nets must have labels and all devices must have distinct names- such as Uxx, where xx is a number, e.g., U00, etc.
4. **Demonstrate** the correct operation of the VME_BIU module **by simulation**. Use real-time (**post-route**) simulations.
5. Turn in a **Project Report**. Your Project Report should include the main sections as follows: Introduction, Design, and Conclusion.

The Class Web Page has pointers to relevant Data Sheets and User's Manuals. Additional materials can be found on the Xilinx, Micron, Digilent and Freescale Home Pages, respectively, and on the other related manufacturers' Web Pages.