

ECE 6050 ADVANCED MICROPROCESSOR APPLICATIONS SPRING 2012

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Class: R 6:30-9:20pm, in C-124, CEAS
Hours: W 5:30-6:20pm, or by appointment

Course Description

The objective of this course is to survey current microprocessors and to discuss various aspects of memory systems design and bus interfacing. Students are expected to have a background in digital logic design and in microprocessor/microcontroller systems design. Though some software topics will also be covered, the primary emphasis will be on hardware design of digital systems and internal architecture of selected processors. The four design projects will be based upon VHDL programming and Field Programmable Gate Arrays (FPGAs). Students will be designing their circuits in VHDL using Xilinx CAD tools (ISE 13.3 and EDK 13.3) along with Modelsim 6.6d by Mentor Graphics. The Xilinx tools and ModelSim are available on PCs located in the Microcomputer Lab (Room B-214). Students are required to download the free Xilinx WebPack 13.3 tools and the free ModelSim PE student version to work on their projects outside of the Microcomputer Lab. The subject matter is considered in the Instructor's Lecture Notes, and in the recommended texts. Additional materials will be posted on the Class Home Page. The Data Sheets of those chips that will be referred to in the design projects can be found in the respective manufacturers' Web sites.

Prerequisites: ECE 5570 Design of Reconfigurable Digital Machines
Permission of the Instructor

Prerequisites by topic: Digital Design
Computer Architecture
Microcontroller Applications

Topics to be covered in this course include:

1. General structure of microprocessors, RISC versus CISC, memory hierarchy, pipelining
2. Static and dynamic RAM memory systems design
3. ARM RISC processor architectures
4. VME/VME64x Bus and interfacing to the VME64x Bus
5. PowerPC-based embedded processors
6. ColdFire processor architectures
7. Motorola 68020/68030/68040/68060 architectures and bus interface
8. Cache coherence with Motorola 68040 processors
9. PCI Bus interface

Required Textbook/Materials

1. Instructor's Lecture Notes, **required**, available through the IEEE Student Branch

2. Data sheets for selected processors, FPGAs, memory and other components. Students are expected to locate and download the needed information from either the vendor's Web site, or from an on-line library.
3. ECE 6050 Parts Kit, **required**. Students can place an order for their Kits by the help of the IEEE Student Branch, or can order the parts by themselves.
4. Most recent versions of the Xilinx WebPack and the ModelSim PE student edition software that can be downloaded from the Xilinx and Mentor Graphics Web sites, respectively, free of charge, **required**.

Recommended Textbook/Materials

1. *Advanced Microprocessors, Second Edition* by Daniel Tabak, McGraw-Hill, 1995, **recommended**, but not required, available in the University Bookstore, Bernhard Center
2. *Microprocessor System Design, Third Edition* by Alan Clements, PWS Publishing Company, 1997, ISBN: 0-534-94822-7, **recommended**, but not required. The Second Edition of the book will be placed on reserve in Waldo Library.
3. Charles H. Roth and Lizy Kurian John, *Digital Systems Design Using VHDL, 2/e*, Cengage Learning, 2008, ISBN 0-534-38462-5, available in the University Bookstore, Bernhard Center.

Course Procedure

There will be **four significant design projects** to be completed. Three projects will be carried on in teams of two students each, or may be worked on individually. Project operational demonstrations must be made to the instructor prior to handing in the written project reports. Project demonstrations and written reports have **firm** due dates for full credit. Projects will be accepted up to three days after due date (not after the last day of the term, though) but will be penalized by the loss of 10% credit for each day late. Failure to work on a project will result in a failing grade for the course. Plagiarism and/or the copying/duplication of another team's design or written reports will result in zero scores for the project for **all** individuals involved.

Grading Policy

Grades will be determined on the following basis:

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|------------------|------------|
| Project 1 | 20% |
| Project 2 | 25% |
| Project 3 | 30% |
| Project 4 | 25% |

It is expected that the breakdown for letter grades will be as follows:

100-91 A, 90-85 BA, 84-75 B, 74-70 CB, 69-61 C, 60-55 D, 54 and below E, missed project E, or X as appropriate. The boundaries between grades may be individually lowered at the instructor's discretion.

Project Due Dates

Project demonstrations will be performed prior to the project due date and time in the Microcomputer Lab (Room B-214). The final, complete written project reports will be due on:

Project 1 6:30pm, Thursday, February 9, 2012

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|------------------|---|
| Project 2 | 6:30pm, Thursday, March 1, 2012 |
| Project 3 | 6:30pm, Thursday, March 29, 2012 |
| Project 4 | 6:30pm, Thursday, April 19, 2012 |

Permission to miss any due date may be granted by the instructor under extreme circumstances. If permission is desired, a request must be made before the due date and should include either a signed doctor's explanation or a written explanation signed by an appropriate WMU officer.

Codes and Policies

The ECE 6050 Web Home Page will be used as official communications media for the class.

The WMU College of Engineering and Applied Sciences Honesty Code will apply in this course.

You are responsible for making yourself aware of and understanding the policies and procedures in the Graduate Catalog that pertain to Academic Honesty. These policies include cheating, fabrication, falsification and forgery, multiple submission, plagiarism, complicity and computer misuse. The instructor will give you guidance to avoid problems of this kind. If there is reason to believe you have been involved in academic dishonesty, you will be referred to the Office of Student Conduct. You will be given the opportunity to review the charge(s). If you believe you are not responsible, you will have the opportunity for a hearing. You should consult with the course instructor if you are uncertain about an issue of academic honesty prior to the submission of an assignment.