

ECE 250 EXAM # 2

Name: _____

Closed book, multiple choice exam. Choose the one best answer.

Lab Section: _____

1. Which of the following will correctly complete the D flip-flop truth table shown below?

D	Q_n	Q_{n+1}	1)	2)	3)	4)	5)
0	0	?	0	0	0	0	1
0	1	?	0	0	1	0	0
1	0	?	1	1	0	0	1
1	1	?	0	1	1	0	0

2. What frequency clock source will produce clock waveforms having a period equal to $0.5\mu\text{sec}$?

- 1) 500 kHz
- 2) 2.0 MHz
- 3) 5 MHz
- 4) .05 MHz
- 5) 2.0 kHz

Note:

μ = micro = 10^{-6}
 m = milli = 10^{-3}
 k = kilo = 10^3
 M = Mega = 10^6

3. Read-Only Memories (ROM's) are constructed from which of the following components?

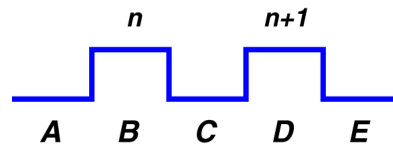
- 1) A DECODER and a MUX
- 2) A MUX and a DEMUX
- 3) A DECODER and an ENCODER
- 4) A MUX and an ENCODER
- 5) A ENCODER and a DEMUX

4. In general, the **Next State** of a sequential logic circuit (SLC) is determined by the:

- 1) MEMORY ELEMENTS
- 2) INPUT LOGIC BLOCK
- 3) OUTPUT LOGIC BLOCK
- 4) INPUTS ONLY
- 5) OUTPUTS ONLY

5. Q_{n+1} is stable over which of the following **clock** regions?

- 1) Region A
- 2) Region B
- 3) Region C
- 4) Region D
- 5) Region E



6. A circuit which translates n input lines into an m bit codeword where $n = 2^m$.

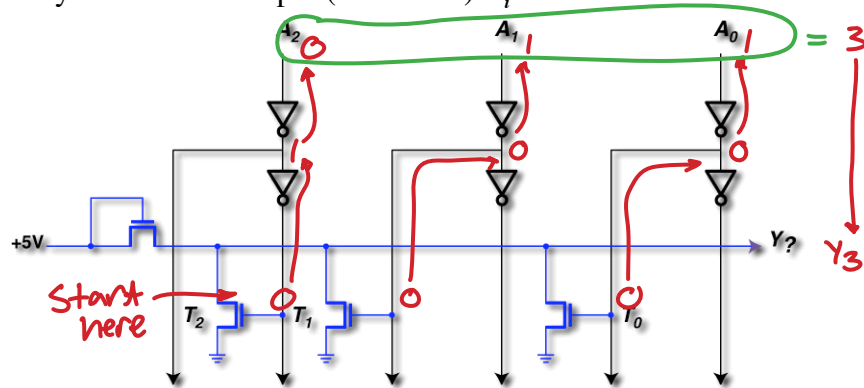
- 1) MUX
- 2) DeMUX
- 3) Decoder
- 4) Encoder
- 5) ROM

7. Which of the following will correctly complete the JK flip-flop truth table shown below?

J	K	Q_n	Q_{n+1}	1)	2)	3)	4)	5)
NC	0	0	0	0	1	1	0	0
R	0	1	0	0	0	1	0	0
S	1	0	0	?	1	0	0	1
T	1	1	0	?	0	1	0	1

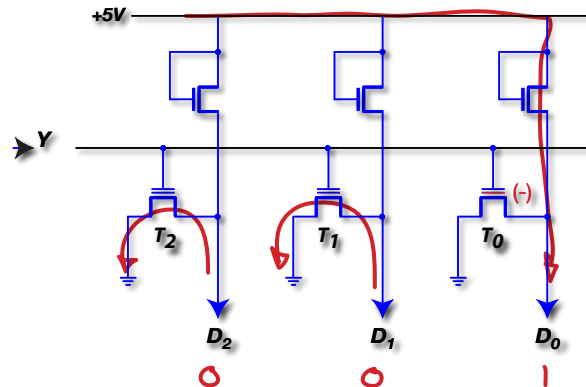
8. Given the (partial) nMOS ROM decoder shown, where $A_2A_1A_0$ are address inputs (A_0 is least significant), identify the decoder output (select line) Y_i :

- 1) $Y = Y_1$
- 2) $Y = Y_2$
- 3) $Y = Y_3$
- 4) $Y = Y_4$
- 5) $Y = Y_5$



9. Given the (partial) nMOS EPROM encoder shown, where Y is some input select line, identify the encoder outputs $D_2D_1D_0$ when $Y = 1$:

- 1) $D_2D_1D_0 = 001$
- 2) $D_2D_1D_0 = 010$
- 3) $D_2D_1D_0 = 111$
- 4) $D_2D_1D_0 = 100$
- 5) $D_2D_1D_0 = 110$



10. The **PRE** and **CLR** inputs of a JK flip-flop set and reset the Q output

- 1) Unconditionally.
- 2) Only after the clock input goes high.
- 3) Only after the clock input goes low.
- 4) Only if $J = 0$ and $K = 0$.
- 5) Only if J and K are not connected to anything.

11. A ROM having a total capacity of **64 K** bits is given. If the ROM is known to have **8** outputs, how many address lines are there?

- 1) 11
- 2) 12
- 3) 13
- 4) 14
- 5) 15 (Note: $K = 1024 = 2^{10}$)

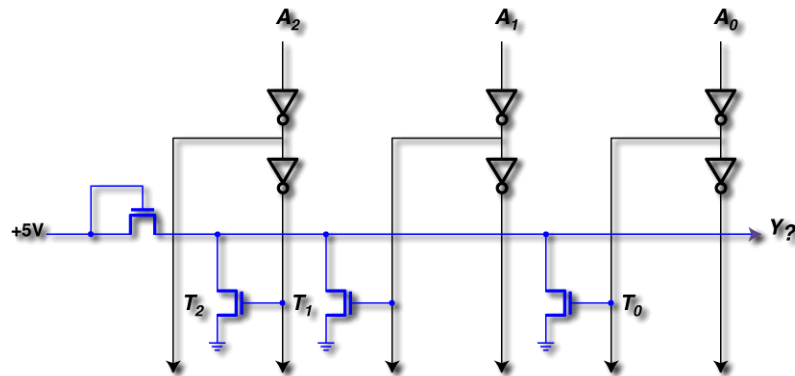
$$\begin{aligned}
 C &= 2^n \times m \\
 64K &= 2^n \times 8 \\
 2^6 \cdot 2^{10} &= 2^n \times 2^3 \\
 \Rightarrow 6+10 &= n+3 \\
 \therefore n &= 13
 \end{aligned}$$

11. Which of the following will correctly complete the JK flip-flop truth table shown below?

J	K	Q_n	Q_{n+1}	1)	2)	3)	4)	5)
0	0	0	?	0	1	1	0	0
0	1	0	?	0	0	1	0	0
1	0	0	?	1	1	0	0	1
1	1	0	?	0	1	1	0	1

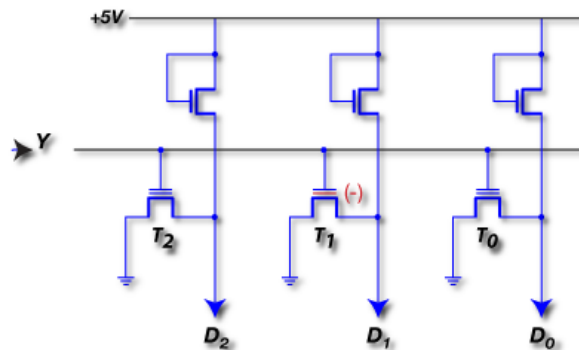
12. Given the (partial) nMOS ROM decoder shown, where $A_2A_1A_0$ are address inputs (A_0 is least significant), identify the decoder output (select line) Y_i :

- 1) $Y = Y_1$
- 2) $Y = Y_2$
- 3) $Y = Y_3$
- 4) $Y = Y_4$
- 5) $Y = Y_5$



13. Given the (partial) nMOS ROM encoder shown, where Y is some input select line, identify the encoder outputs $D_2D_1D_0$ when $Y = 1$:

- 1) $D_2D_1D_0 = 001$
- 2) $D_2D_1D_0 = 010$
- 3) $D_2D_1D_0 = 111$
- 4) $D_2D_1D_0 = 100$
- 5) $D_2D_1D_0 = 110$



14. The **PRE** and **CLR** inputs of a JK flip-flop set and reset the **Q** output

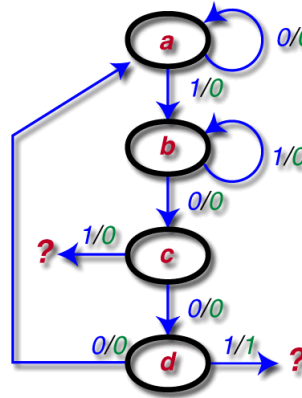
- 1) Unconditionally.
- 2) Only after the clock input goes high.
- 3) Only after the clock input goes low.
- 4) Only if $J = 0$ and $K = 0$.
- 5) Only if J and K are not connected to anything.

15. A ROM having a total capacity of **32 K** bits is given. If the ROM is known to have **8** outputs, how many address lines are there?

- 1) 11
- 2) 12
- 3) 13
- 4) 14
- 5) 15 (Note: $K = 1024 = 2^{10}$)

16. Where should the left and right arrows be directed in order that the state diagram illustrated detect the sequence $X = 1001$ with overlap?

- 1) Left: **b** Right: **b**
- 2) Left: **c** Right: **b**
- 3) Left: **b** Right: **a**
- 4) Left: **a** Right: **d**
- 5) Left: **a** Right: **a**



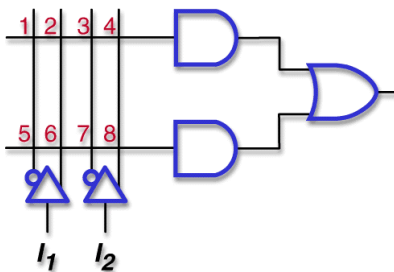
17. What is the logic equation for the output Z for the state diagram of the previous question, if the following state assignments (Y_1Y_2) are given: $a = 00, b = 01, c = 10, d = 11$.

- 1) $Z = \overline{X}Y_1\overline{Y_2}$
- 2) $Z = XY_1Y_2$
- 3) $Z = XY_1\overline{Y_2}$
- 4) $Z = \overline{X}Y_1\overline{Y_2}$
- 5) $Z = \overline{X}Y_1Y_2$

18. What is the purpose of state c of the state diagram of the previous question?

- 1) To remember that the most previous input was a 1.
- 2) To remember that the most previous input was a 0.
- 3) To remember that the two most previous inputs were 10.
- 4) To remember that the two most previous inputs were 11.
- 5) To remember that the three most previous inputs were 101.

19. Indicate the programming connections required (1 to 8) to implement an **AND** function using the **PLD AND array** shown below:



- 1) 1, 7, 6, 8
- 2) 2, 4, 5, 6
- 3) 2, 4 (only)
- 4) 5, 7
- 5) 5, 7, 1, 2

20. Given the state table below, the output sequence generated by an input sequence $X = 1000110$ and starting state **d** is

- 1) $Z = 0011110$
- 2) $Z = 0111011$
- 3) $Z = 0011001$
- 4) $Z = 0110100$
- 5) $Z = 0111001$

Note:
PS = Present State
X = Input
NS = Next State
Z = Output

PS	X	NS	Z
a	0	a	1
a	1	b	0
b	0	a	0
b	1	c	0
c	0	c	1
c	1	d	1
d	0	b	1
d	1	a	0