

Closed book, multiple choice exam. Choose the one best answer.

Lab Section: Form A

1. Where should the left and right arrows be directed in order that the state diagram illustrated below detect the sequence  $X = 1001$  with overlap?

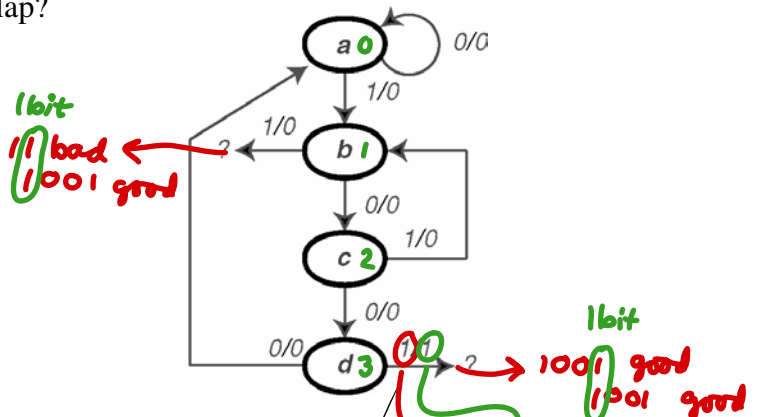
1) Left: c Right: b

2) Left: b Right: b

3) Left: b Right: a

4) Left: a Right: d

5) Left: a Right: a



2. What is the logic equation for the output  $Z$  for the state diagram of the previous question, if the following state assignments  $(Y_1, Y_2)$  are given:  $a = 00, b = 10, c = 11, d = 01$  →  $Y_1, Y_2 = 01, X = 1$

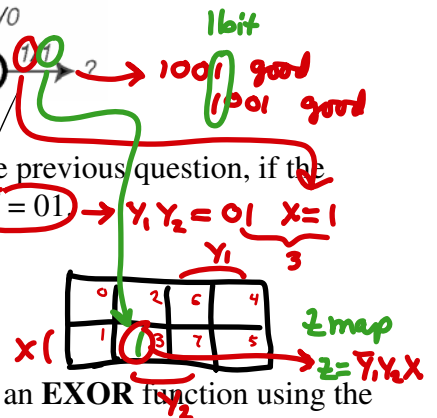
1)  $Z = \bar{X} \bar{Y}_1 \bar{Y}_2$

2)  $Z = X Y_1 \bar{Y}_2$

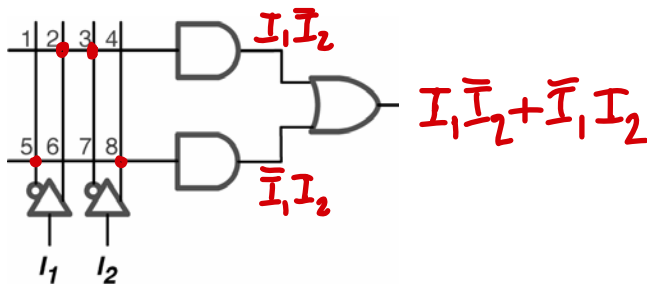
3)  $Z = X \bar{Y}_1 Y_2$

4)  $Z = \bar{X} Y_1 \bar{Y}_2$

5)  $Z = X Y_1 Y_2$



3. Indicate the programming connections required (1 to 8) to implement an EXOR function using the PLD AND array shown below:



1) 1, 2, 3, 4

2) 2, 3, 5, 8

3) 5, 7, 2, 4

4) 3, 4, 7, 8

5) 1, 3, 6, 8

4. Given the state table below, the output sequence generated by an input sequence  $X = 0111000$  and starting state **b** is

1)  $Z = 0111011$

2)  $Z = 1001001$

3)  $Z = 0110010$

4)  $Z = 0010111$

5)  $Z = 1001100$

Note:

PS = Present State

X = Input

NS = Next State

Z = Output

PS	X	NS	Z
a	0	b	1
a	1	c	1
b	0	d	0
b	1	a	1
c	0	d	1
c	1	d	0
d	0	c	1
d	1	a	0

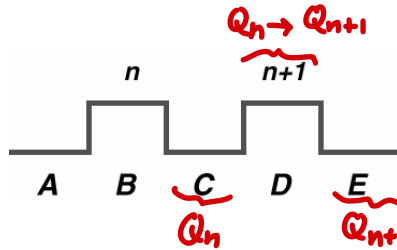
$X = 0111000$   
 $Y = b \rightarrow a \rightarrow c \rightarrow d \rightarrow c \rightarrow d$   
 $Z = 0010111$

5. In general, the *Next State* of a sequential logic circuit is determined by the:

- See picture file*
- 1) MEMORY ELEMENTS
  - 2) INPUT LOGIC BLOCK
  - 3) OUTPUT LOGIC BLOCK
  - 4) INPUTS only
  - 5) OUTPUTS only

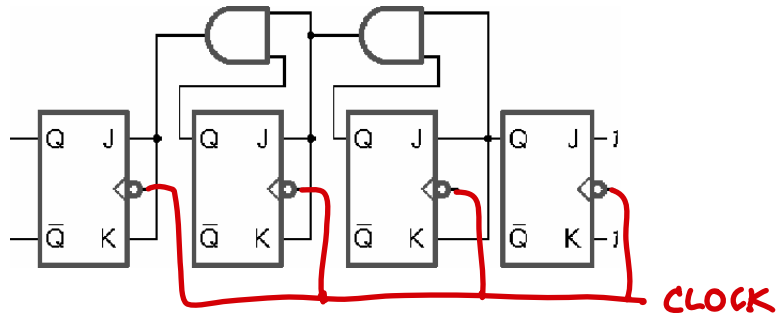
6.  $Q_n > Q_{n+1}$  over which of the following clock regions?

- 1) Region A
- 2) Region B
- 3) Region C
- 4) Region D
- 5) Region E



7. The sequential logic circuit shown below represents most closely the basic architecture of a:

- 1) Data-latch register
- 2) Ripple counter
- 3) Synchronous counter
- 4) Shift register
- 5) Up/Down counter

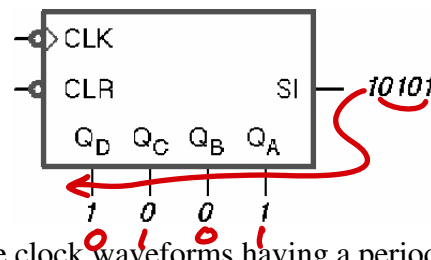


8. A circuit which translates n input lines into a m-bit code word is defined as a

- 1) MUX
  - 2) DeMUX
  - 3) Decoder
  - 4) Encoder
  - 5) ROM
- See notes*

9. If  $Q_D Q_C Q_B Q_A = 1001$  initially, what are the contents of the shift register below after the input sequence  $SI = 10101$  is applied? (Assume 5 clock pulses are used.)

- 1) 1111
- 2) 1011
- 3) 0101
- 4) 1010
- 5) 1001



10. What frequency clock source will produce clock waveforms having a period equal to  $2.0\mu\text{sec}$ ?

- 1) 50 kHz
- 2) 2.0 MHz
- 3) 2 kHz
- 4) .05 MHz
- 5) 500 kHz

$T = 2\mu\text{sec}$

$$f = \frac{1}{T} = \frac{1}{2 \times 10^{-6} \text{ sec}}$$

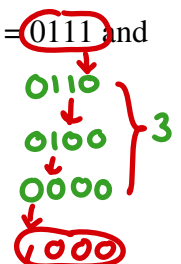
$$= \frac{1}{2} \times \frac{1}{10^{-6}} \times \frac{1}{\text{sec}}$$

$$= .5 \times 10^6 \text{ Hz} = 500 \times 10^3 \text{ Hz} = 500 \text{ kHz}$$

Note:  
 $\mu = \text{micro} = 10^{-6}$   
 $m = \text{milli} = 10^{-3}$   
 $k = \text{kilo} = 10^3$   
 $M = \text{Mega} = 10^6$

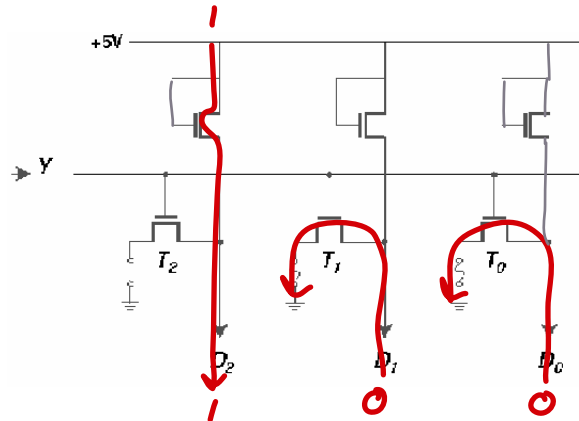
11. How many transient states does a 4-bit ripple counter transit through between count = 0111 and count = 1000?

- 1) one
- 2) two
- 3) three
- 4) four
- 5) none



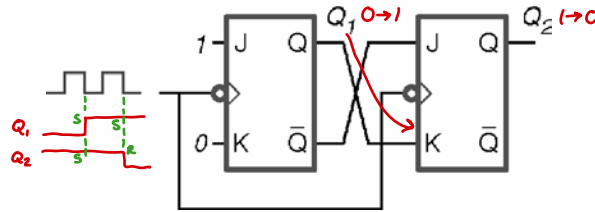
12. Given the (partial) nMOS ROM encoder shown, where  $Y$  is some input select line, identify the encoder outputs  $D_2 D_1 D_0$  when  $Y = 1$ :

- 1)  $D_2 D_1 D_0 = 0 0 0$
- 2)  $D_2 D_1 D_0 = 1 1 1$
- 3)  $D_2 D_1 D_0 = 0 1 1$
- 4)  $D_2 D_1 D_0 = 1 1 0$
- 5)  $D_2 D_1 D_0 = 1 0 0$

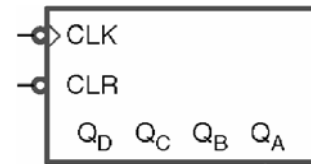
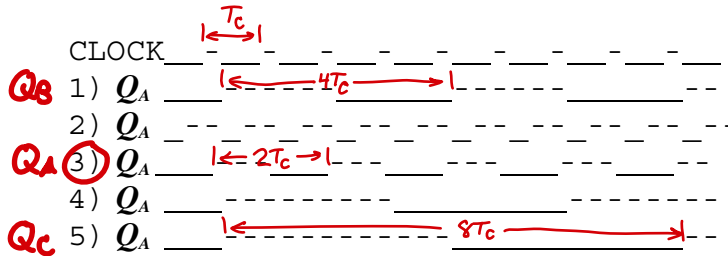


13. Suppose  $Q_1 = 0$  and  $Q_2 = 1$  is the initial state of the two flip-flop (M/S) circuit shown. What is the state of the circuit after application of two complete clock pulses to the first flip-flop?

- 1)  $Q_1 = 0, Q_2 = 0$
- 2)  $Q_1 = 0, Q_2 = 1$
- 3)  $Q_1 = 1, Q_2 = 0$
- 4)  $Q_1 = 1, Q_2 = 1$



14. Which of the following waveforms can be generated by the output  $Q_A$  of the synchronous counter shown? ( $Q_A$  is least significant)



15. Which of the following will correctly complete the JK flip-flop truth table shown below?

	J	K	$Q_n$	$Q_{n+1}$	1)	2)	3)	4)	5)
NC	0	0	1	1	0	1	1	0	1
R	0	1	1	0	0	0	1	1	1
S	1	0	0	1	1	1	0	0	0
T	1	1	0	1	1	1	1	1	0

16. A ROM having a capacity of 16 K and 8 outputs is given. How many address lines are there?

- 1) 11
  - 2) 12
  - 3) 13
  - 4) 14
  - 5) 15
- (Note:  $K = 1024 = 2^{10}$ )

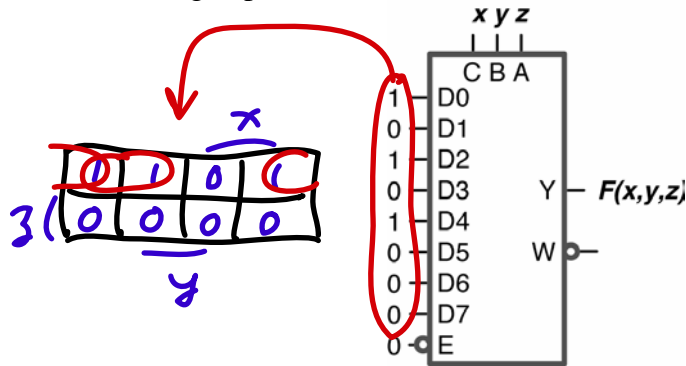
$$C = 2^n \times m$$

$$16K = 2^n \times 8$$

$$2^4 \cdot 2^{10} = 2^n \times 2^3 \rightarrow 4 + 10 = n + 3 \rightarrow n = 11$$

17. An 8 to 1 MUX is connected as shown, where  $x, y$  and  $z$  are inputs ( $z$  is least significant) and  $F$  is a output. Which of the following expressions correctly describes  $F$  ?

- 1)  $F = \bar{x}y + x\bar{z}$
- 2)  $F = \bar{x}y + y\bar{z}$
- 3)  $F = \bar{x}\bar{y} + \bar{x}\bar{z}$
- 4)  $F = \bar{y}z + y\bar{z}$
- 5)  $F = \bar{x}\bar{z} + \bar{y}\bar{z}$



18. The **PRE** and **CLR** inputs of a master/slave JK flip-flop set and reset the  $Q$  output

- 1) Unconditionally. *See notes*
- 2) Only after the clock input goes high.
- 3) Only after the clock input goes low.
- 4) Only if  $J = 0$  and  $K = 0$ .
- 5) Only if  $J$  and  $K$  are not connected to anything.

19. Which of the following best describes how to construct a **1 to 8 demultiplexer** from a 3 to 8 decoder:

- 1) Connect the decoder input select lines **CBA** to  $D$ .
- 2) Connect the decoder enable input to  $D$ . *See notes*
- 3) Connect the decoder input data lines all to  $D_i$ .
- 4) Connect the  $i$ th decoder output to  $D_i$ .
- 5) Connect  $Y$  to  $D$  and  $W$  to  $\bar{D}$

20. Given the variables  $Y_{1n}, Y_{2n}$ , and input  $X$ , which of the following represent the correct contents of the  $K_1$  K-map given the next state map  $Y_{1n+1}$ ?

	$Y_{1n+1}$ :		$Y_{1n}$	
	1	0	1	1
$X$	1	0	0	1

	$K_1$ :		$Y_{2n}$	
	d	d	0	0
$X$	d	d	1	0
			$Y_{1n}$	

- 1) d d 1 1
- 2) 1 d d 1
- 3) d d 0 0
- 4) d 1 0 d
- 5) 0 d d 0