Laboratory Ten

Sequential Logic Circuit Design

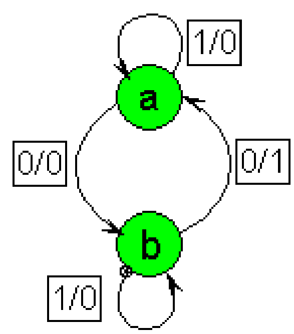
Basic Concepts

The design of a sequential logic circuit (SLC) in our class involves the application of the following 5 step procedure discussed in the lecture:

1. The first step in designing a SLC is to draw a *block diagram* (which identifies inputs and outputs) and a *state diagram* (which specifies the relationship between inputs, outputs and states).
2. The second step involves deriving a *state table* which tabulate inputs, present states, next states and outputs. The states are also encoded to binary in this step.
3. In step 3 the *next state* and *output maps* are filled in.
4. In step 4, you need to decide whether to use either **D** or **JK** flip-flops for the circuit implementation. **D** or **JK** maps are then derived.
5. Finally in step 5, Boolean equations are derived from the **D** or **JK** maps plus **Z** maps, and circuits are drawn.

Note: This prelab is worth 10 points.

Task One: A Simple 2-State SLC



1. (Pre) Draw a block diagram for the SLC described by the state diagram shown at right, which utilizes input ***X***, state variable ***Y*** and output ***Z***. Also include a ***RESET*** input for clearing the circuit. See the lecture *example*.
2. (Pre) Draw a state table for the 2-state SLC.
3. (Pre) Derive, using steps 3-5 of the procedure outlined above, a suitable circuit to realize this system using **JK** flip-flops and gates. In your work, assume that state ***a*** is the *reset* state (***Y*** = 0) and state ***b*** is the *set* state ***Y*** = 1.
4. Your lab instructor shall now give you a short section of ***ABEL*** code (a simpler language, similar to ***VHDL***) to model your SLC in ***Xilinx***, using a single **JK** flip-flop.
5. Simulate the circuit in **Xilinx**. For your test waveforms, apply an input sequence of ***X = 111000110*** and plot waveforms for both ***Y*** and ***Z***. (Make sure to apply one short ***RESET*** pulse sometime during the first three **ones** of ***X***). For what state and input does ***Z = 1***?
6. Download your design to the Digilent board, using proper PINs for the ***X***, ***RESET*** and ***CLOCK*** inputs, and the **LED** bar graph for displaying ***Y*** and ***Z***.
7. Now exercise the inputs according to your timing diagram and record the observed ***Y*** and ***Z*** output pattern in your notebook (along with ***X*** and ***CLOCK***). How well did the waveforms follow the simulation?
8. Is the SLC a **Mealy** or **Moore** machine?

Task Two: Bimodal Counter Design

Consider the design of a *bimodal counter*. This counter has two modes (bimode) of operation and three flip-flops. The first mode of operation is called *run* (where the counter "counts") and the second mode is called *wait* (where the counter holds and the count does not change). Assume that input $M = 0$ puts the counter in the *wait* mode and $M = 1$ starts the *run* mode. A ***RESET*** signal is also required to clear out the counter.

1. (Pre) To begin, draw a block diagram for a bimodal 4-state counter, identifying inputs, state variables and outputs. Derive also a state diagram for this 4-state SLC. Refer to the 5 step procedure outlined for the *4-state counter example*, discussed in the lecture.
2. (Pre) Draw a state table for the 4-state SLC, following the example given in class.
3. (Pre) Derive, using steps 3-5 once again, a suitable circuit to realize this system using the **JK** flip-flops and gates. Assume your states will have codes 00 to 11.
4. (Pre) Examining your 2 flip-flop, 4-state counter circuit, let's see how we can extend it to a 3-flip-flop, 8-state counter. Draw a third flip-flop right above the Y_1 flip-flop and label its Q output as Y_0. Now, noticing that J_1 and K_1 are driven by an AND gate whose output is MY_2, connect the J_0 and K_0 of the new third flip-flop to second AND gate producing the signal MY_1Y_2. Connect the ***CLOCK*** and ***RESET***. Done!
5. Model your 3 flip-flop counter circuit in ***ABEL***.
6. Simulate your design and test it using an input test sequence of your own design. Demonstrate your testing scheme with your instructor.
7. Download your design to the Digilent board.
8. Finally, exercise the inputs according to your timing diagram and record the observed Y output pattern in your notebook. How well does it follow the simulation?
9. Is the SLC a **Mealy** or **Moore** machine?