Laboratory Nine - Continued

Flip-Flops and Registers

Basic Concepts

1. A flip-flop is a binary storage element designed specifically to work with a clock signal (CLOCK). There are 2 basic types of flip-flops, the D (data) flip-flop and the JK flip-flop. Flip-flops are designed to make state changes only on the rising or falling edges of the CLOCK.
2. A shift register consists of a string of D flip-flops, which are able to exchange data with their nearest neighbors. It is typically constructed from D flip-flops.
3. The traditional counter consists of a string of JK flip-flops. It is typically constructed from JK flip-flops operating in the toggle mode.

Note: This prelab assignment is worth 10 points. Lab is still 10.

Task One: The D Flip-Flop

1. (Pre) Review your D-latch results from last week, and draw the waveforms CLOCK, D and RESET, and record the resulting Q output changes, keeping in mind that state changes can only be performed on the rising edge of the CLOCK. Mark the mode of operation (Set or Reset only) above each clock edge (see dotted lines below).
2. Construct the Logisim D flip-flop testing circuit shown at right. In this circuit, the CLOCK and D inputs are derived from switches (which can be set high or low), and the RESET input comes from a push-button, which produces a high only when depressing the button. Please leave the “1” and “en” inputs unconnected.
3. While RESET is set high, construct a truth table that illustrates the D F/F properties, having inputs D and Qn and output Qn+1.
4. Now, exercise the CLOCK and D inputs to the flip-flop according to your waveform signals. To begin, clear the Q output by pressing the RESET button.
Task Two: The JK Flip-Flop

1. (Pre) Draw the timing diagram shown below for the JK flip-flop having waveforms CLOCK, J, K, and output Q. Mark the mode of operation (NC, Set, Reset, Toggle) performed on each rising edge of the clock shown below.

2. Construct the Logisim JK flip-flop testing circuit shown at right. In this circuit, the J and K inputs are connected to switches while the CLOCK and RESET inputs both come from push-buttons.

3. While RESET is high in the flip-flop, construct a truth table that illustrates the JK flip-flop properties, having inputs J, K, Q, and output Qn+1.

4. Put the flip-flop in toggle mode and explain what happens each time you press the debounced switch.

5. Exercise the RESET, CLOCK and JK inputs of the JK flip-flop according to the waveforms below. Record the resulting responses.
Task Three: 8-Bit Shift Register

A shift register consists of a string of D flip-flops, which are able to exchange data with their nearest neighbors, as seen by the red paths below. The serial input (SI) determines what the first D flip-flop in the string will receive. 2-to-1 MUXes help also to allow both left and right shifting, or a parallel load.

1. A Shift Register can be modeled in Logisim as shown below, using MUXes to allow both right and left shifts. The memory elements used in this case are D flip-flops which shift data one bit position per clock pulse. Build the 8-bit shift register in Logisim and perform the following tests:
   a. Set \( R_{in} \) high for 8 clocks and fill-up the register.
   b. Set \( L_{in} \) low for 8 clocks and empty the register.
   c. Set \( R_{in} \) high for one clock to send a solitary high-bit left or right down the register.

2. Redesign the shift register of Step 1 so it can accept a parallel load from 8 data inputs A-H on the top, while still allowing right shifts. Control this again by the Dir signal, (but now relabel the Dir signal as the LOAD signal.) Also include a CLEAR input (not shown) routed to all flip-flops.

3. Simulate your results (for just the first 4 bit positions A-D) using the sample waveforms shown below showing input waveforms Clock, CLEAR, SI (serial-input \( R_{in} \)), LOAD (synchronously load parallel inputs), A-D (parallel inputs) and blank output waveforms \( Q_A-Q_D \).
Task Four: The 74163 4-bit Counter

We will now look at the 74163 TTL 4-bit counter, a counter that was designed with a lot of functionality in the 1960's.

1. Please mount and wire up the 74163 MSI counter on the blue box. Verify that your counter counts. The CLOCK input must use the debounced push-down buttons on the red box and the Q outputs should be connected to LEDs.

2. Repeat the counting action using an ordinary non-debounced switch for the clocking signal. You should see some skipped numbers. Explain why the counter skips some numbers when counting up.

3. Complete the 74163 timing diagram shown below for the input waveforms CLOCK, LOAD (synchronous-load), and the (blank) output waveforms Q0-Qa. (The RC output shall be ignored.) Note that in the 74163, CLEAR and LOAD are active-low and synchronous to the CLOCK.

4. Use the clock signal CLK provided by the WaveGen, 5V square wave at 1kHz to exercise the 74163. The logic analyzer setup is:
   a. D100-D103 connected to A-D counter outputs
   b. D106 connected to CLK
   c. D107 connected to RCO output pin
   Which should yield the waveforms at bottom below.