To illustrate the frequency response design of a phase-lag compensator, consider the following SMD positioning system controlled by the compensator \( G_c(s) \). Here, \( X_d(s) \) and \( X(s) \) are the desired and actual positions of the mass.

Proportional control (\( G_c(s) = K \)): Large gains are required to control steady-state error to a step input. Unfortunately, large gains produce undesirable, oscillatory closed-loop response. Below, we design a phase-lag compensator to lower the steady-state error without introducing highly oscillatory behavior.

**Problem:** Design a phase-lag compensator so the closed-loop system has a steady-state position error \( e_{ss} = 1 - x_{ss} < 0.1 \) to a unit step input and a phase margin \( PM = 45 \) (deg). Plot the step response of the resulting closed-loop system.

**Frequency Response Design**  
**M-file:** PhaseLagPositionControlSMDwithBode.m

**Step 1:** Determine the compensator gain required to satisfy the error specification.

The steady state error can be defined in terms of the loop transfer function as

\[
e_{ss} = \lim_{s \to 0} \left[ \frac{1}{1 + GH(s)} \right] = \frac{1}{1 + \frac{K}{2}} = \frac{1}{1 + K_p} < 0.1
\]

So, \( K_p > 9 \) and \( K > 18 \).

**Step 2:** Evaluate the phase margin of the uncompensated system with \( K = 18 \).

Using MATLAB, the phase margin of this (the uncompensated system) is \( PM \approx 28 \) (deg). See plot below. This is well below the desired phase margin.
Step 3: Locate the zero of the compensator

By examination of the Bode diagram, we see that the phase margin requirement would be satisfied at 2.74 (rad/sec). This statement assumes the magnitude plot crosses over the zero dB line at this point. So, we locate the zero of the compensator at least one decade below this frequency, for example, at 0.25 (rad/sec).

Step 4: Locate the pole of the compensator

To make 2.74 (rad/s) the zero dB crossover point, we require approximately 8 dB of attenuation from the compensator. (See Bode plot of uncompensated system.) We now calculate $\alpha$ by setting $-8 = 20\log(\alpha)$ to find $\alpha = 0.3981$. Our first iteration yields the compensator

$$G_c(s) = 0.3981 \left[ \frac{s + 0.25}{s + 0.0995} \right]$$

(Phase-lag compensator)

Step 5: Check the phase margin of the new compensated system.

The Bode diagram of the loop transfer function of the compensated system

$$GH(s) = 0.3981 \left[ \frac{s + 0.25}{s + 0.0995} \right] \left[ \frac{18}{s^2 + 2s + 2} \right]$$

shows that the phase margin is $PM = 43.7$ (deg), satisfying the original requirement.
Step 6: Repeat steps 3-5 until the desired phase margin is obtained.

Our compensated system nearly meets the specification. We will use this result.

Step 7: Check the step response.

Step response of the uncompensated system shows a large overshoot (about 49%) and low damping (settling time of 3.78 seconds), while the step response of the phase lag compensated system shows a smaller overshoot (around 22%) with higher damping and a longer settling time of 7.7 seconds. So, the reduction of overshoot comes at the price of increasing the settling time.

Step Response of Compensated System has less overshoot and more damping than the Uncompensated System. Unfortunately, it also has a longer settling time. This is typical of integrator-type compensators.
**Frequency Response of Compensated Closed Loop System:**

The frequency response of the closed loop system is shown below. The *bandwidth* of the closed loop system is approximately 4 (rad/s).