Antti-Aliasing Filter Design
ECE 3200 Electronics II
version 19 February 2022

References
2. W. H. Middendorf and R. H. Engelmann, *Design of Devices and Systems*, Marcel Dekker, 3rd ed., 1998. This is the current text for the ECE Senior Design Sequence. In that class you will explore design methods to turn specifications (what the device is supposed to do) to parameters (information to build the device that meets the specs, e.g. schematics and component values).

Objectives
1. Generate and validate a design based on a set of specifications as a member of an engineering design team.
2. To improve and further develop an ability to effectively communicate technical information via a written report.

Pre-Laboratory Assignment
(ONE PRE-LAB ASSIGNMENT PER GROUP — WORK TOGETHER)

A power electronics system requires sampling a zero-average 2V peak-to-peak 60Hz sinusoid using an A/D converter. The available A/D converter has a maximum sampling rate of 10kHz with a resolution of 16 bits over a range of 0-1V. A maximally-flat low pass filter using the fewest components with at least 60dB attenuation for frequencies above the Nyquist frequency is required. You must use the full range of the A/D converter and +/-9V DC supplies are available. Due to an IC shortage, only 741 op-amps are available. You must only use standard resistor and component values available in the ECE 3200 lab as listed in previous labs.

1. The prelab must include a Team Member Contributions that describes how tasks were assigned and completed to meet the objective of producing a preliminary design.
2. List and number the design specifications, that is, what the circuit is supposed to do.
4. Design your anti-aliasing circuit. Provide an LTspice® simulation that demonstrates that your design “works”. Use a table to show if the design meets the required specifications:

<table>
<thead>
<tr>
<th>Specification #</th>
<th>Specification met?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. XYZ</td>
<td></td>
</tr>
</tbody>
</table>

5. You must find the transfer function of the filter section. Use LTspice® to plot the transfer function magnitude (the example of Figure 1 will be helpful) and compare to the filter circuit Bode magnitude plot.
6. Compute the resolution and quantization error of your system (in mV).
**Procedures**

1. Construct and validate your circuit.

Your lab report must include a table in the summary that indicates whether each specification was met and how verified:

<table>
<thead>
<tr>
<th>Specification #</th>
<th>Specification met?</th>
<th>How verified</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. X Y Z</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The summary must also indicate whether the design was successful. Justify.

The “best” design (including documentation) will earn a coveted ECE 3200 *Best Design Award*.

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