ECE 3200 Electronics II
Summer I 2012
EXAM 2

NAME: ____________________________________________

INSTRUCTIONS:

1. **THIS EXAM IS CLOSED BOOK AND CLOSED NOTES** other than one-side of a 3"x5" note card. Write your name on the unused side of the card. **Turn your card in with the exam.**

2. You may use an approved calculator; **NO OTHER ELECTRONIC DEVICES ARE ALLOWED.**

   **CALCULATOR MANUFACTURER:** ____________________
   
   **CALCULATOR MODEL:** ______________________________

3. Work each problem in the provided space.

4. Show **ALL work required to arrive at a solution for either full or partial credit.**

5. **READ the entire question before answering.**

6. **CIRCLE YOUR ANSWERS.**

7. Have your student ID on your desktop for inspection by the instructor.

8. **SIGN the honesty pledge at the bottom of the page. Exams without a signature will receive no credit.**

I have neither given nor received assistance from anyone in regards to completion of this exam. I have followed the instructions as provided on this sheet.

**SIGNATURE:** _______________________________ **DATE:** __________

References


Note: some problems might be adapted from the course text or other sources. Schematics prepared using LTspice IV (linear.com). © 2012 Damon A. Miller
Maximum exam score is 45 points.

1. (5 points) Using a graph, illustrate why the transconductance $g_m$ of an NMOS transistor is POSITIVE and the transconductance $g_m$ of a PMOS transistor is NEGATIVE.

2. (5 points) Using a graph, illustrate the effect of the Early voltage $V_A = \frac{1}{\lambda}$ on the $i_D$ vs. $v_{DS}$ curves for a NMOS transistor.
3. (5 points) Consider the following circuit (adapted directly from [1]). Assume that the meter reads $V_M = 9V$. What is the MOSFET threshold voltage $V_{th}$? Carefully justify your answer using a graph.
4. (15 points) Consider the following circuit adapted directly from [1]. Assume that the transistors are in the saturation region.

   a. Conduct a DC analysis. Assume the transistors are matched. Find the DC voltages at nodes A, B, C, D, and E. Note that \( k_n = k_p = 1 \text{ mA/V}^2 \) (includes W/L), \( V_{tn} = 1 \text{ V} \), and \( V_{tp} = -1 \text{ V} \). Ignore the channel-length modulation effect (\( \lambda = 0 \)).

   b. Draw the small signal equivalent circuit assuming that the capacitors are shorts at the frequencies of interest and ignoring the channel-length modulation effect (\( \lambda = 0 \)).

   c. Find the small signal voltage gain \( \frac{v_d}{v_i} \).
5. (15 points) Consider the following circuit adapted from [1] where

\[
\begin{align*}
\frac{W}{L}_8 &= \frac{W}{L}_5 = \frac{W}{L}_7 = \frac{W}{L}_1 = \frac{W}{L}_2 = \frac{W}{L}_3 = \frac{W}{L}_4 = 1 \quad \text{and} \quad \frac{W}{L}_6 = 2.
\end{align*}
\]

Assume that the transistors are in the saturation region, \(k'_n = k'_p = 1 \text{ mA/V}^2\) (does NOT include W/L), \(V_{tn} = 1 \text{ V}\), and \(V_{tp} = -1 \text{ V}\). Find the small signal voltage gain \(v_f/\nu_{id}\) where \(\nu_{id} = (\nu_a - \nu_b)\). Ignore the channel-length modulation effect (\(\lambda=0\)) in the DC analysis. For the AC analysis let \(|\lambda|=1/(50\text{ V})\).