ECE 3200 Electronics II
Spring 2018
FINAL EXAM

NAME: _____

INSTRUCTIONS:

1. **THIS EXAM IS CLOSED BOOK AND CLOSED NOTES** other than one-side of a 3"x5" note card. Write your name on the unused side of the card. **Turn your card in with the exam.**
2. **YOU MAY USE ONE OF THESE CALCULATORS.**
   Circle the one, if any, that you are using:

   Casio fx-115/fx-991

   HP 33s/35s

   TI 30X/36X
3. **All other electronic devices must be stowed away**.
4. Work each problem in the provided space.
5. Show ALL work required to arrive at a solution for either full or partial credit.
6. READ the entire question before answering.
7. Have your student ID on your desktop for inspection by the instructor.
8. SIGN the honesty pledge at the bottom of the page. Exams without a signature will receive no credit.

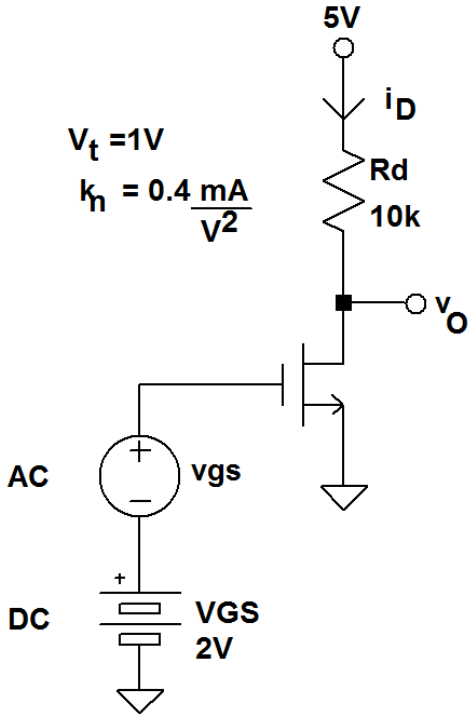
I have neither given nor received assistance from anyone in regards to completion of this exam.
I have followed the instructions as provided on this sheet.
I have verified that the exam has (7) pages.

SIGNATURE: _____ DATE: _____

Note: some problems might be adapted from the course text or other sources. Schematics prepared using LTspice® (linear.com).

Maximum exam score is 40/30 (problem 4 is worth (10) points extra credit).

1. Consider the following circuit.
   Ignore λ.
   a. (2 points) Find the Q point (I_D, V_{DS}).
   b. (2 points) Verify that the transistor is in the saturation region.
   c. (4 points) Draw the small-signal equivalent circuit diagram.
   d. (2 points) Use (c) to find the small signal voltage gain.



Adapted directly from: Sedra and Smith, Microelectronic Circuits, 4th ed.

EXTRA WORK SPACE FOR PROBLEM 1

2. (10 points) Consider the following CMOS op-amp circuit. Find the small-signal voltage gain

$$v_f/v_{id} = \{g_{m1}(r_{02}||r_{o4})\}\{-g_{m6}(r_{06}||r_{o7})\}$$

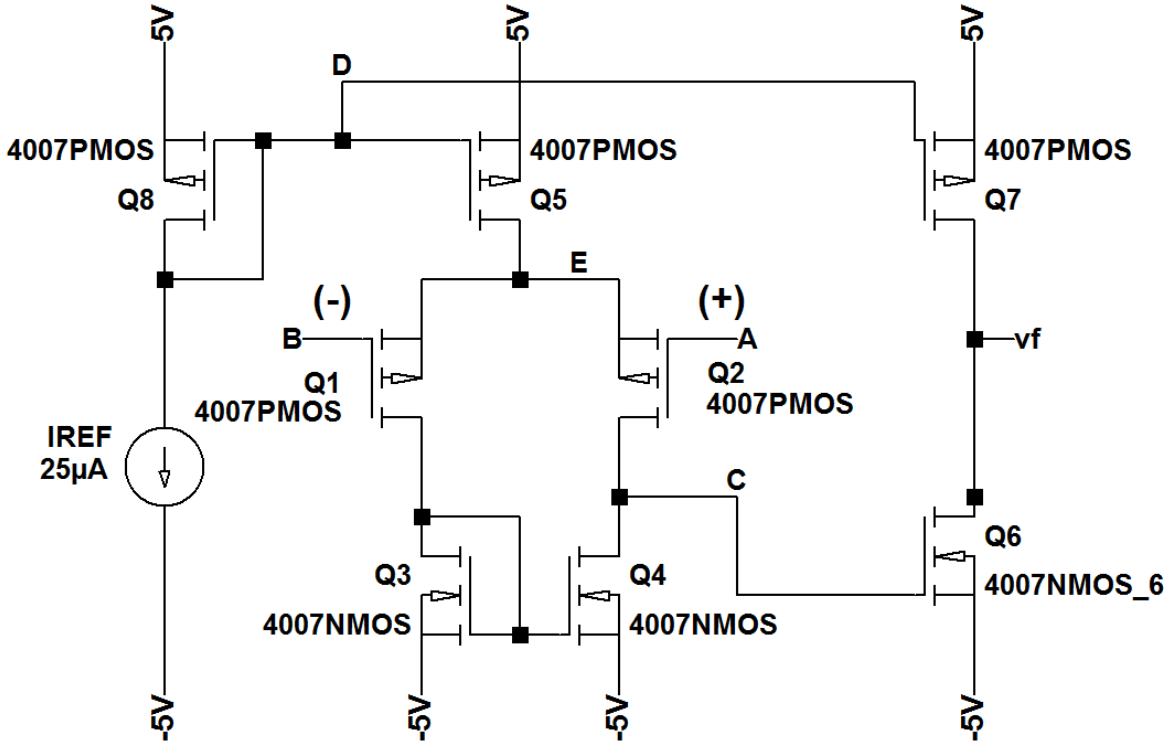
where $v_{id} = (v_a - v_b)$.

Assume that the transistors are in the saturation region. Also:

- $k_n' = 20$ μA/V^2 (does NOT include W/L)
- $k_p' = 10$ μA/V^2 (does NOT include W/L)

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	120/8	120/8	50/10	50/10	150/10	100/10	150/10	150/10

- $V_{tn} = 1$V and $V_{tp} = -1$V
- Ignore the channel-length modulation effect (λ=0) in any DC computations.
- $V_{An} = |V_{Ap}| = 25$V



Adapted directly from Sedra and Smith, Microelectronic Circuits, 4th ed.

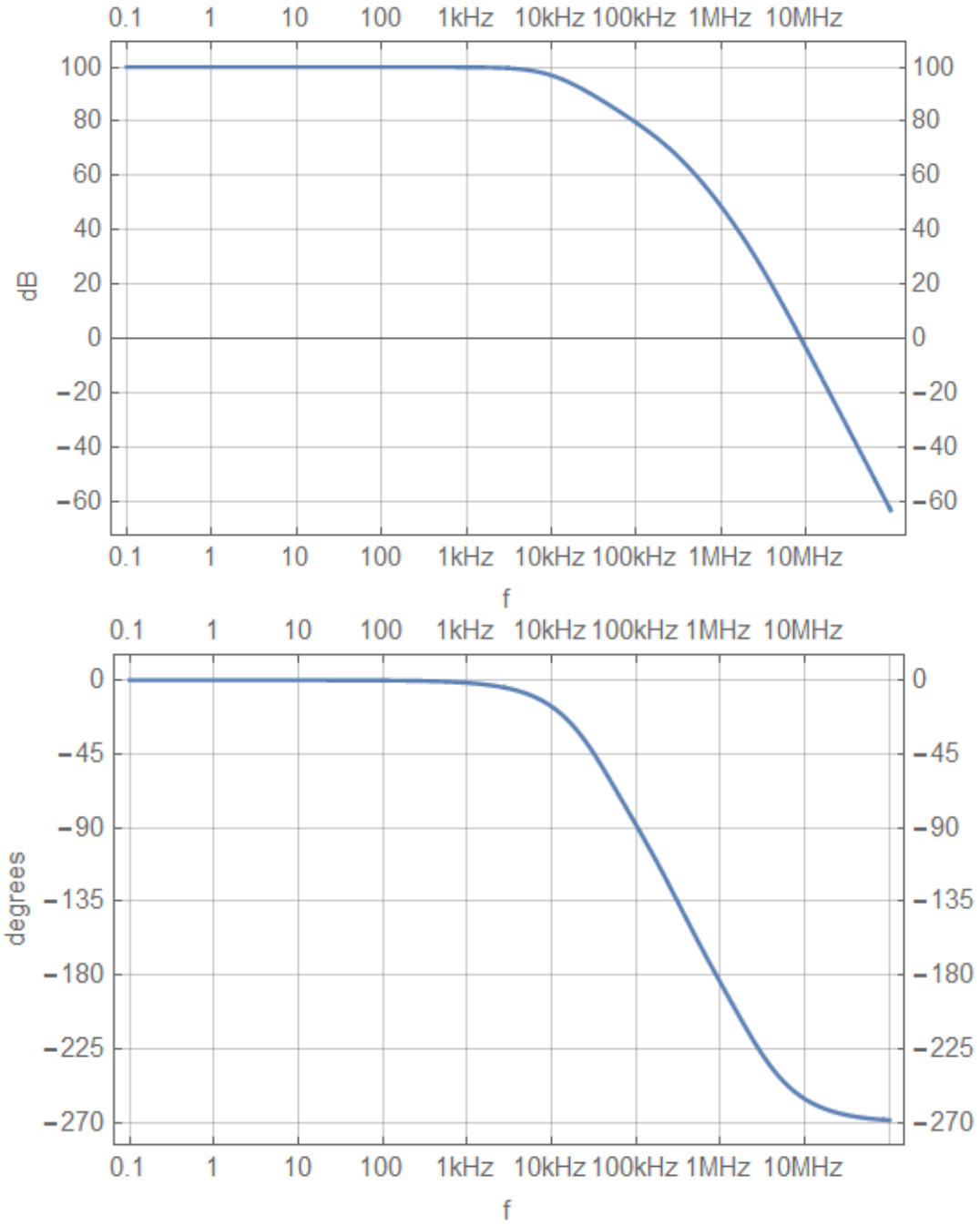
EXTRA WORK SPACE FOR PROBLEM 2

3. (10 points) An operational amplifier has the following open-loop gain and phase characteristics. Note that the poles are at 10kHz, 316kHz, and 2.2MHz.

   a. Using the plots ESTIMATE the minimum stable closed-loop gain.

   b. Using the plots ESTIMATE the closed-loop gain that has a phase margin of 45 degrees.

   c. Using the plots ESTIMATE a new frequency for the **first pole at 10kHz** so the operational amplifier can be used in a unity feedback circuit.



4. (10 points, EXTRA CREDIT) Use an ideal op-amp, one capacitor, and two resistors to design a low pass filter with a low frequency gain of 20dB and a -3dB frequency of 1MHz.

   Provide a Bode magnitude plot for your circuit.