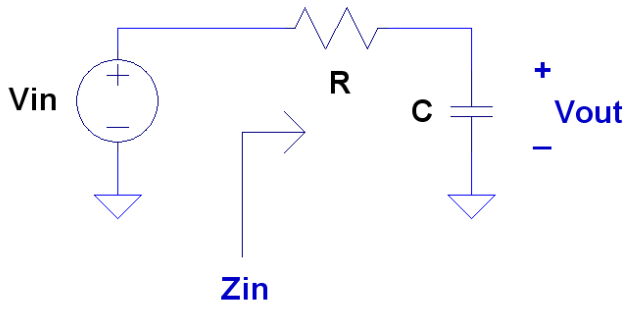
ECE4810

PRACTICE PROBLEM 10.100

Consider a series RC circuit (drawn using LTspice IV):



The circuit is to be designed to have a specified input resistance magnitude $||\boldsymbol{Z}in||$ at $\omega=2\pi$ (60 Hz) rad/s and a specified output voltage $Vout=a$ at $t=1$ ms for a unit step input voltage at $t=0$.

1. Describe how the device evolution design "method" could be applied to this problem and why you would not want to use this approach in this case.
2. Using the repeated analysis design method with the SPICE engine of your choice, find the parameters R and C such that $||\boldsymbol{Z}in||=1000\Omega$ and $Vout(1\text{ ms})=0.5$V for a unit step input voltage at $t=0$.
3. Develop a synthesis procedure to find the parameters R and C given $||\boldsymbol{Z}in||$ and $Vout(1\text{ ms})=a$ for a unit step input voltage at $t=0$. Verify your synthesis procedure by applying it to the specifications of part (2).
4. Find a set of specifications that will result in a physically unrealizable design.

Carefully document your work. Attach a signed statement stating that your results have been verified and are correct. Assignments will not be accepted without this statement.

Reference

W. H. Middendorf and R. H. Engelmann, Design of Devices and Systems, Marcel Dekker, 3rd ed., 1998