ECE 4500/5540 DIGITAL ELECTRONICS  
Fall 2016 Laboratory Session Outline

Lab Instructor: Mohammed Al-Gailani  
Meeting times: TR 6:30pm – 9:00pm in Laboratory B-210  
Office hours: will be posted on the Class Home Page  
Email: mohammedyasser.algailani@wmich.edu  
Lab Assignments: have been posted on the Class Home Page  
Pre-lab Assignments: will be posted on the Class Home Page

Lab Work

The lab will cover nine experiments, one of them being a two-session lab. Lab work will be done in teams of two students to develop skills for collaboration. However, the course instructor may assign three students or just one student to a team. Team assignments will be decided by the course instructor and will be posted on the Class Web Page. Starting with Lab 2, students are required to complete pre-lab assignments. This will enable students to make full use of the available lab time. Students are also expected to take advantage of the swipe card access to the B-210 Lab.

Students will be using the Mentor Graphics EDA tools. These tools run under Linux OS inside the VMW virtual machine. At the end of each lab session students must save all their work on their thumb-drives and are required to delete the files from their work folders on the hard drives in the B-210 Lab. This is to prevent even accidental plagiarism in the lab. Teams are required to submit an electronic copy (.pdf) lab report for each lab (but for Lab 1) to the Lab TA via the appropriate Drop Box in Elearning. Lab Reports are due on the day before the next lab at 5:00pm, i.e., at 5:00pm, on Monday (ECE 4500 and ECE 5540-105 Section) and at 5:00pm, on Wednesday (ECE 5540-100 Section). Late submissions will be penalized by 15% credit per day the report is tardy. Reports will NOT be accepted after 3 days of the due date.

Before a new lab starts (Lab 3 to Lab 9), students are required to run the DRC check and the LVS checks on both the overall design and the cell level design, respectively, of the prior lab and show the results to the Lab TA. The Lab TA will review the full designs to make sure that the teams have actually completed the previous lab before starting a new one. After the verification of the results of the prior lab is done students will present their pre-labs for the new lab to the Lab TA.

If you do not show up for a lab, you will not be given any points for that lab. There will be no make up labs. Exceptions will be only made for students who have provided adequate reasons, and who have given a notice at least a day in advance to the Lab TA that they cannot attend the lab that day. Students have to achieve a passing grade in the lab (60% out of 100%) in order to pass the class.

Starting with Lab 3, bonus credits may be given to one team (one undergraduate and one graduate, respectively) who have produced a complete and high-quality lab report and met the criteria of the most efficient design (details will be given by the Lab TA). Decisions on the bonus credits will be made by considering the product of the layout size and the two propagation delays (should be at minimum), as well as the quality of the simulation results.
for the assigned design. Bonus credits may not be given to any team if all requirements are not met.

The **ECE 4500 and ECE 5540-105 Lab Final Exams** will be given *6:30-9:10pm, on Tuesday, November 22, 2016*, while the **ECE 5540-100 Lab Final Exam** will be given *6:30-9:10pm, on Thursday, December 1, 2016*, respectively. The time frame will be split into two sessions. In each session a different test problem will be assigned. Students will have about 1 hour and 10 minutes to complete the test. **Sign-up sheets** for the Lab Final sessions will be posted approx. one week before the Lab Final.

**Grading**

Lab work: 20% of the course grade  
Each lab (Labs 2 to 9): 13 points, out of which is up to 3 points for the pre-lab assignment (104 points total)  
Lab Final: 39 points  
Lab bonuses (Labs 3 to 9): 12 points max. (2 points max. per lab)  
**Note:** Grades will be posted weekly on the Class Web Site.

**Report format for the .pdf files**  
**(No hand written work except comments on simulation results)**  
1. Front cover  
2. Lab description and design approach (not more than one page)  
3. Schematic Design (Circuit diagram – Design Architect)  
4. Eldo Simulations/Xelga Viewer – Pre-layout timing diagrams  
   - Suitable input stimuli  
   - DC Sweep (if needed)  
   - Propagation delays (t_{plh} and t_{phl})  
   - Performance calculations (based upon the t_{plh} and t_{phl} values obtained via simulation)  
5. IC Layout – Layout Graphics  
6. LVS report (important!)  
7. Calibre-based Post Layout DRC checks  
8. Calibre-based Post Layout LVS report (upper level cell check necessary)  
9. Conclusion  
   - Transistor count  
   - IC layout area  
   - Propagation delays (t_{phl} and t_{plh})  
   - **Product** of the layout size and the propagation delays (the potential extra credit will be primarily given on the grounds of this value).

**Lab report score break up (may change based upon the assigned tasks)**

Schematic design: 10%  
Eldo simulations (pre-layout): 40%  
IC Layout: 40%  
Calibre reports (DRC checks and LVS report, assuming the IC level is correct): 10%
Honesty Code

The ECE 4500/5540 Web Home Page will be used as official communications media for the class. Students must check the Home Page on a daily basis.

The WMU College of Engineering and Applied Sciences Honesty Code will apply in this course.

Students are responsible for making themselves aware of and understanding the University policies and procedures that pertain to Academic Honesty. These policies include cheating, fabrication, falsification and forgery, multiple submission, plagiarism, complicity and computer misuse. The academic policies addressing Student Rights and Responsibilities can be found in the Undergraduate Catalog at http://catalog.wmich.edu/content.php?catoid=24&navoid=974 and the Graduate Catalog at http://catalog.wmich.edu/content.php?catoid=25&navoid=1030. If there is reason to believe you have been involved in academic dishonesty, you will be referred to the Office of Student Conduct. You will be given the opportunity to review the charge(s) and if you believe you are not responsible, you will have the opportunity for a hearing. You should consult with your instructor if you are uncertain about an issue of academic honesty prior to the submission of an assignment or test.

Students and instructors are responsible for making themselves aware of and abiding by the “Western Michigan University Sexual and Gender-Based Harassment and Violence, Intimate Partner Violence, and Stalking Policy and Procedures” related to prohibited sexual misconduct under Title IX, the Clery Act and the Violence Against Women Act (VAWA) and Campus Safe. Under this policy, responsible employees (including instructors) are required to report claims of sexual misconduct to the Title IX Coordinator or designee (located in the Office of Institutional Equity). Responsible employees are not confidential resources. For a complete list of resources and more information about the policy see www.wmich.edu/sexualmisconduct.

In addition, students are encouraged to access the Code of Conduct, as well as resources and general academic policies on such issues as diversity, religious observance, and student disabilities:

Office of Student Conduct www.wmich.edu/conduct

Division of Student Affairs www.wmich.edu/students/diversity

University Relations Office http://www.wmich.edu/policies/religious-observances-policy

Disability Services for Students www.wmich.edu/disabilityservices